Description of Control Signals in our Single Cycle Implementation of the RISC-V 32I ISA

| Signal Name | # of bits | value | action |
|--------------------|--------------|-------|---|
| PCMux.CTL | 2 | 0 | Next PC = output of ALU |
| | | 1 | Next PC = result of branch instruction |
| | | 2 | Next PC = PC + $(targ20 \ll 1)$ |
| | | 3 | Next PC = PC + 4 |
| regFile.WE | 1 | 0 | Register file not written |
| | | 1 | Register file written: rd will be updated with value of the write input |
| regInputMux.CTL | 3 | 0 | Write Input = ALU output |
| | | 1 | Write Input = 4-bytes from Data Memory |
| | | 2 | Write Input = sext 2-bytes from data memory |
| | | 3 | Write Input = sext 1 byte from data memory |
| | | 4 | Write Input = PC + value based on PCAddMux.CTL |
| PCAddMux.CTL | 1 | 0 | Send 4 + PC towards registers |
| | | 1 | Send (I[31:12] << 12) + PC towards regs |
| DATA.WE | 4 | 0 | Data memory not written |
| | | 1 | [0001] write the least significant byte from source register to data memory |
| | | 3 | [0011] write the two lower bytes from source register to data memory |
| | | 15 | [1111] write all four bytes of the source register to data memory |
| ALUInputMux.CTL | 1 | 0 | Second input to ALU is rs2 |
| | | 1 | Second input to ALU is I[31:0] |
| ALU.CTL | 6 | | |
| Arithmetic Ops (I) | | 0 | C = A + se(B[31:20]) |
| | | 1 | C = A < se(B[31:20]) ? 1 : 0 |
| | | 2 | C = A < unsigned se(B[31:20]) ? 1 : 0 |
| | | 3 | C = A ^ se(B[31:20]) |
| | | 4 | C = A se(B[31:20]) |

| | 5 | C = A & se(B[31:20]) |
|--------------------|----|---------------------------------------|
| | 6 | C = A << se(B[24:20]) |
| | 7 | C = A >> se(B[24:20]) |
| | 8 | C = A >>> se(B[24:20]) |
| Arithmetic Ops (R) | 9 | C = A + B |
| | 10 | C = A - B |
| | 11 | C = A << B[4:0] |
| | 12 | C = A < signed B ? 1 : 0 |
| | 13 | C = A < unsigned B ? 1 : 0 |
| | 14 | $C = A \wedge B$ |
| | 15 | C = A >> B[4:0] |
| | 16 | C = A >>> B[4:0] |
| | 17 | $C = A \mid B$ |
| | 18 | C = A & B |
| Comparator Ops | 19 | C = A == B ? 1 : 0 |
| | 20 | C = A != B ? 1 : 0 |
| | 21 | C = A < signed B ? 1 : 0 |
| | 22 | C = A >= signed B ? 1 : 0 |
| | 23 | C = A < unsigned B ? 1 : 0 |
| | 24 | C = A >= unsigned B ? 1 : 0 |
| Multiplication Ops | 25 | C = (A * B) [31:0] |
| | 26 | C = (signed(A) * signed(B))[63:32] |
| | 27 | C = (signed(A) * unsign(B))[63:32] |
| | 28 | C = (unsign(A) * unsign(B))[63:32] |
| Division Ops | 29 | C = A /signed B |
| | 30 | C = A /unsign B |
| | 31 | C = A %signed B |
| | 32 | C = A %unsign B |
| Misc | 33 | C = B[31:12] << 12 |
| | 34 | C = A + se(B[31:20]) & ~0x1 |
| | 35 | C = (B[31]B[19:12]B[20]B[30:21]) << 1 |
| | 36 | C = A + se(B[31:25]B[11:7]) |