RISC-V RV32IM ISA Reference Sheet v1.4

31 25	24 20	19 15	14 12	11 7	6 0	
funct7	rs2	rs1	funct3	rd	opcode	R-type
imm[11:0]		rs1	funct3	rd	opcode	I-type
imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode	S-type
imm[12,10:5]	rs2	rs1	funct3	imm[4:1,11]	opcode	B-type
imm[31:12]				rd	opcode	U-type
imm[20,10:1,11,19:12]				rd	opcode	J-type

instruction		fmt	opcode	fun3	fun7	semantics	encoding
lui	rd,imm20	U	0x37			rd = imm20 << 12	iiii iiii iiii iiii iiii dddd d011 0111
auipc	rd,imm20	U	0x17			rd = pc + (imm20 << 12)	iiii iiii iiii iiii iiii dddd d001 0111
addi	rd,rs1,imm12	I	0x13	000		rd = rs1 + se(imm12)	iiii iiii iiii ssss s000 dddd d001 0011
slti	rd,rs1,imm12	I	0x13	010		rd = rs1 <signed se(imm12) ? 1 : 0	iiii iiii iiii ssss s010 dddd d001 0011
sltiu	rd,rs1,imm12	I	0x13	011		rd = rs1 <unsign se(imm12) ? 1 : 0	iiii iiii iiii ssss s011 dddd d001 0011
xori	rd,rs1,imm12	I	0x13	100		rd = rs1 ^ se(imm12)	iiii iiii iiii ssss s100 dddd d001 0011
ori	rd,rs1,imm12	I	0x13	110		rd = rs1 | se(imm12)	iiii iiii iiii ssss s110 dddd d001 0011
andi	rd,rs1,imm12	I	0x13	111		rd = rs1 & se(imm12)	iiii iiii iiii ssss s111 dddd d001 0011
slli	rd,rs1,imm12	I	0x13	001	0x0	rd = rs1 << imm12[4:0]	0000 000i iiii ssss s001 dddd d001 0011
srli	rd,rs1,imm12	I	0x13	101	0x0	rd = rs1 >> imm12[4:0]	0000 000i iiii ssss s101 dddd d001 0011
srai	rd,rs1,imm12	I	0x13	101	0x20	rd = rs1 >>> imm12[4:0]	0100 000i iiii ssss s101 dddd d001 0011
add	rd,rs1,rs2	R	0x33	000	0x0	rd = rs1 + rs2	0000 000t tttt ssss s000 dddd d011 0011
sub	rd,rs1,rs2	R	0x33	000	0x20	rd = rs1 - rs2	0100 000t tttt ssss s000 dddd d011 0011
sll	rd,rs1,rs2	R	0x33	001	0x0	rd = rs1 << rs2[4:0]	0000 000t tttt ssss s001 dddd d011 0011
slt	rd,rs1,rs2	R	0x33	010	0x0	rd = rs1 <signed rs2 ? 1 : 0	0000 000t tttt ssss s010 dddd d011 0011
sltu	rd,rs1,rs2	R	0x33	011	0x0	rd = rs1 <unsign rs2 ? 1 : 0	0000 000t tttt ssss s011 dddd d011 0011
xor	rd,rs1,rs2	R	0x33	100	0x0	rd = rs1 ^ rs2	0000 000t tttt ssss s100 dddd d011 0011
srl	rd,rs1,rs2	R	0x33	101	0x0	rd = rs1 >> rs2[4:0]	0000 000t tttt ssss s101 dddd d011 0011
sra	rd,rs1,rs2	R	0x33	101	0x20	rd = rs1 >>> rs2[4:0]	0100 000t tttt ssss s101 dddd d011 0011
or	rd,rs1,rs2	R	0x33	110	0x0	rd = rs1 | rs2	0000 000t tttt ssss s110 dddd d011 0011
and	rd,rs1,rs2	R	0x33	111	0x0	rd = rs1 & rs2	0000 000t tttt ssss s111 dddd d011 0011
lb	rd,imm12(rs1)	I	0x03	000		rd = se(mem[rs1+se(imm12)][7:0])	iiii iiii iiii ssss s000 dddd d000 0011
lh	rd,imm12(rs1)	I	0x03	001		rd = se(mem[rs1+se(imm12)][15:0])	iiii iiii iiii ssss s001 dddd d000 0011
lw	rd,imm12(rs1)	I	0x03	010		rd = mem[rs1+se(imm12)][31:0]	iiii iiii iiii ssss s010 dddd d000 0011
lbu	rd,imm12(rs1)	I	0x03	100		rd = ze(mem[rs1+se(imm12)][7:0])	iiii iiii iiii ssss s100 dddd d000 0011
lhu	rd,imm12(rs1)	I	0x03	101		rd = ze(mem[rs1+se(imm12)][15:0])	iiii iiii iiii ssss s101 dddd d000 0011
sb	rs2,imm12(rs1)	S	0x23	000		mem[rs1+se(imm12)][7:0] = rs2[7:0]	iiii iiit tttt ssss s000 iiii i010 0011
sh	rs2,imm12(rs1)	S	0x23	001		mem[rs1+se(imm12)][15:0] = rs2[15:0]	iiii iiit tttt ssss s001 iiii i010 0011
sw	rs2,imm12(rs1)	S	0x23	010		mem[rs1+se(imm12)][31:0] = rs2	iiii iiit tttt ssss s010 iiii i010 0011
jal	rd,targ20	J	0x6f			rd = pc+4; pc += se(targ20<<1)	iiii iiii iiii iiii iiii dddd d110 1111
jalr	rd,imm12(rs1)	I	0x67	000		rd = pc+4; pc = (rs1+se(imm12)) & ~0x1	iiii iiii iiii ssss s000 dddd d110 0111

beq rs1,rs2,targ12	B	0x63	000		if (rs1 == rs2) pc += se(targ12<<1)	iiii iiit tttt ssss s000 iiii i110 0011
bne rs1,rs2,targ12	B	0x63	001		if (rs1 != rs2) pc += se(targ12<<1)	iiii iiit tttt ssss s001 iiii i110 0011
blt rs1,rs2,targ12	B	0x63	100		if (rs1 <signed rs2) pc += se(targ12<<1)	iiii iiit tttt ssss s100 iiii i110 0011
bge rs1,rs2,targ12	B	0x63	101		if (rs1 ≥signed rs2) pc += se(targ12<<1)	iiii iiit tttt ssss s101 iiii i110 0011
bltu rs1,rs2,targ12	B	0x63	110		if (rs1 <unsign rs2) pc += se(targ12<<1)	iiii iiit tttt ssss s110 iiii i110 0011
bgeu rs1,rs2,targ12	B	0x63	111		if (rs1 ≥unsign rs2) pc += se(targ12<<1)	iiii iiit tttt ssss s111 iiii i110 0011
mul rd,rs1,rs2	R	0x33	000	0x01	rd = (rs1 * rs2)[31:0]	0000 001t tttt ssss s000 dddd d011 0011
mulh rd,rs1,rs2	R	0x33	001	0x01	rd = (signed(rs1) * signed(rs2))[63:32]	0000 001t tttt ssss s001 dddd d011 0011
mulhsu rd,rs1,rs2	R	0x33	010	0x01	rd = (signed(rs1) * unsign(rs2))[63:32]	0000 001t tttt ssss s010 dddd d011 0011
mulhu rd,rs1,rs2	R	0x33	011	0x01	rd = (unsign(rs1) * unsign(rs2))[63:32]	0000 001t tttt ssss s011 dddd d011 0011
div rd,rs1,rs2	R	0x33	100	0x01	rd = rs1 /signed rs2	0000 001t tttt ssss s100 dddd d011 0011
divu rd,rs1,rs2	R	0x33	101	0x01	rd = rs1 /unsign rs2	0000 001t tttt ssss s101 dddd d011 0011
rem rd,rs1,rs2	R	0x33	110	0x01	rd = rs1 %signed rs2	0000 001t tttt ssss s110 dddd d011 0011
remu rd,rs1,rs2	R	0x33	111	0x01	rd = rs1 %unsign rs2	0000 001t tttt ssss s111 dddd d011 0011