CIS 2400 Fall 2024 - Second Written Homework

Assignment Instructions:

You will submit this assignment by uploading it to Gradescope. You do not need to print out this document and put your answers on it. You should probably instead put your answers on their own dedicated pages, and then properly indicate which question is being answered on all parts of each page.

You may write your answers and draw them by hand or type them and use an online program to draw the circuits. Whatever you do, please make sure your circuit is clear and readable. If you are drawing by hand, a straight-edge and/or graph paper may help with readability.

Please also note that this homework is graded manually and does not have "public test cases" like the other homeworks usually will have. **It also means that we will not grant late extensions that exceed 72 hours aside from special circumstances.**

5 problems: 100 pts total

Problem 1 (15 pts)

Design a single CMOS transistor circuit that has 2 inputs, A and B and produces a high output if and only if A is high (A = 1) and B is low (B = 0). In order to accomplish this, you can assume that you also have access to the inverses of A and B and that you can use those as inputs to your circuit. Please remember that to get full points your circuit must be a proper CMOS circuit, label the pull down and pull up networks and make sure that these two circuits are complementary to each other.

Problem 2 (20 pts)
Design a single CMOS transistor circuit that has 3 inputs, A, B and C, that represents a 3-bit unsigned integer where A is the MSB, B is the middle bit, and C is the LSB. For example, if the input was equivalent to the integer value 3 (0b011), A would be 0, B would be 1 and C would be 1. The circuit should produce a high output if and only if the unsigned integer value is a multiple of 3. 0, 3 and 6 are the possible multiples of 3 that can occur with a 3-bit unsigned integer.

In order to accomplish this, you can assume that you also have access to the inverses of A, B and C and that you can use those as inputs to your circuit. Please remember that to get full points your circuit must be a proper CMOS circuit, label the pull down and pull up networks and make sure that these two circuits are complementary to each other.

Problem 3
Consider the following boolean function that takes 3 inputs (A, B, C): Output = (A OR B) AND C.

Problem 3a (10 pts)
Design a single CMOS transistor circuit that has 3 inputs, A, B and C that implements the boolean function: Output = (A OR B) AND C.

In order to accomplish this, you can assume that you also have access to the inverses of A, B and C and that you can use those as inputs to your circuit. Please remember that to get full points your circuit must be a proper CMOS circuit, label the pull down and pull up networks and make sure that these two circuits are complementary to each other.

Problem 3b (10 pts)
Implement a gate-level circuit that has 3 inputs, A, B and C that implements the boolean function: Output = (A OR B) AND C. Be sure to properly label all inputs and outputs to the circuit and make sure you are drawing a readable & legal gate level circuit

Problem 3c (10 pts)
In class we briefly went over the pros and cons of working at different abstraction levels. These can include things like development time, readability, transistor delay, cost, etc. If you had to regularly design circuits as part of your job, which abstraction level (CMOS-level or Gate-level) would you want to work with? Please briefly explain your reasoning in 2-3 sentences.

(Note: the choice here is subjective, so we care about your explanation for your choice)

Problem 4 (15 pts)
Design a PLA circuit that takes a 4 bit input, I, representing a 4 bit unsigned number and outputs a logical 1 if and only if the input is a power of 2 (e.g., 1, 2, 4, 8). Please make sure to clearly label your diagram to indicate which signal lines represent the four inputs: I3, I2, I1, and I0 where I3 corresponds to the MSB of the input and I0 to the LSB.

(please refer to the course slides for a description of a PLA circuit, it's a gate level circuit with one layer of AND gates and a final OR gate that implements a sum of products function directly).

Problem 5 (20 pts)
Design a logic circuit in class (similar to the saturation adders we did in class before fall break) that implements a conditional add. In particular we have three inputs P, A, B and C, each of which are a 4-bit unsigned integer. The circuit has one output that is represented by a 4-bit unsigned integer. If A and B are equal, then output should be P + C. If A and B are NOT equal, then output should be P + 4.

Please label your diagram clearly: Label the inputs, outputs, relevant intermediate values and make sure you are clear about which wires are multi-bit like we did in class with the saturated adders.

You are allowed to use the 4-bit Adder we developed in class, Mux, and any of the basic logic gates (NOT, AND, OR, NAND, NOR, XOR, XNOR). You are also allowed to refer to specific bits of each input (e.g. A is made up of A3, A2, A1 and A0, where A3 is the most significant bit, and A0 is the least significant bit). We suggest looking at what we did in class for the saturation adders to get some inspiration.