CIS 2400 Fall 2024 - Homework #6

Assignment Instructions:

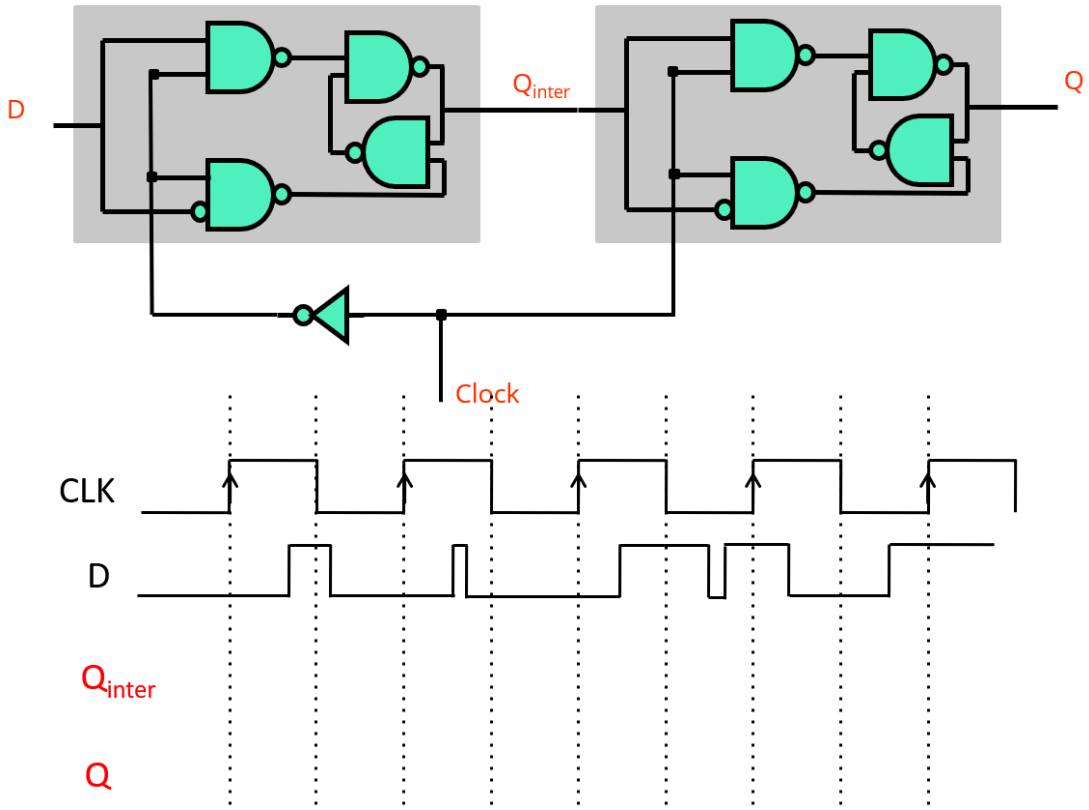
You will submit this assignment by uploading it to Gradescope. You do not need to print out this document and put your answers on it, and may instead put your answers on their own dedicated pages, just be sure you properly indicate which question is being answered on all parts of the page.

You may write your answers and draw them by hand or type them and use an online program to draw the circuits. Whatever you do, please make sure your circuit is clear and readable. If you are drawing by hand, a straight-edge and/or graph paper may help with readability.

Please also note that this homework is graded manually and does not have "public test cases" like the other homeworks usually will have. **It also means that we will not grant late extensions that exceed 72 hours aside from special circumstances.**

Problem 1 (10 pts)

In class we discussed the D Flip-Flop and showed a timing diagram for that device. In the figure below we have replicated that diagram but have changed the input signal D. Your job is to complete the timing diagram by filling in the Q and Q_{inter} signals assuming that they were both low before the first rising edge of the clock shown:



Problem 2 (30 pts)
In the class slides we described a 3-bit counter that would count up from 0 to 7 then repeat. This is a classic example of a finite state machine. On each clock cycle the value stored in the 3-bit register was incremented from the output of a 3 bit incrementer circuit which was itself composed of a chain of 1 bit incrementer units. For this problem you are going to design a 4 bit circuit that counts down instead of up, that is the value on the 4 bit register when viewed as an unsigned integer should change as follows on each clock cycle : …4,3,2,1,0,15,14,13,12,11,….

Part 1: 16 points. First you must design a 4-bit decrementer circuit that takes in a 4 bit number and outputs that value minus 1. This circuit can be constructed using the same idea that we used for the incrementer circuit, that is it can be constructed from a chain of identical units. Explain how to do this then provide a gate level design of what goes in each of the units in the same way that the 1 bit incrementer blocks were expanded into gates in the notes.

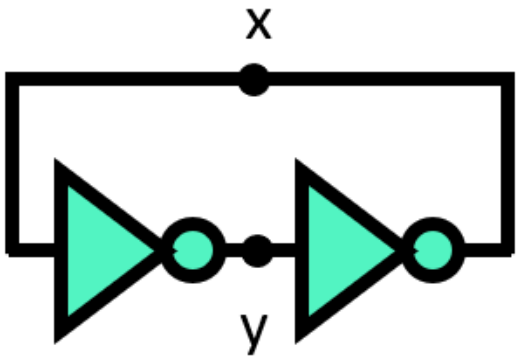
Part 2: 7 points. Once you have designed your 4-bit decrementer circuit you must provide a schematic of the 4 bit count down circuit. Your schematic should show each of the 4 flip flops and how their inputs and outputs are connected to the units in the decrementer circuit. Please indicate which flip flop stores the MSB and which the LSB. You can draw each D-flip flop as a box labeled Dff. Do not forget to draw the clock and WE signals, though WE can be left out of the drawings if it is clearly stated that it is always high.

Part 3: 7 points. Produce a new variant of your design that acts as an up/down counter. This circuit has one additional input called UP/DN. If this input is zero the value on the 4 bit register should go up by one on the next rising edge. If it is 1 the value should go down by 1. You can assume that this UP/DN input signal is stable before the next rising edge. You should be able to do this by modifying slightly the circuit you produced for the previous part. You can assume that you have access to the 1-bit incrementer mentioned in lecture.

Problem 3 (20 pts)

Part 1: 5 points

Consider the circuit below consisting of a ring of 2 inverters. You can assume that each inverter has a gate delay of 1ns. Assume both y and x started with a low voltage “0”. Explain how the signal at the point labeled X would change over a 12 ns period using a timing diagram. Make sure to indicate the time duration of any relevant sections on your diagram and that it is clear when a signal is high versus low.



Part 2: 5 points

What happens if we assume that the wire x starts at a low voltage "0" and y starts at a high voltage “1”? Show how the signal at the point labeled X would change over a 12 ns period using a timing diagram. You can assume that each inverter has a gate delay of 1ns.

Part 3: 10 points

How would your answer change if we increased the number of inverters to 3 as shown below? You should assume that each inverter has a gate delay of 1ns, that x starts at a low voltage “0”, y starts at a low voltage “0”, and z starts with a high voltage “1”. Show your answer using a time diagram that shows how the signal at the point labeled X would change over a 12 ns period.