University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE3700, Spring 2024 Final Tuesday, May 7

- Problem weightings shown.
- Calculators allowed.
- Closed book = No text or notes allowed.
- Additional workspace in exam book. Note where to find work in exam book if relevant.

Name:

Q1	
Q2	
Q3	
Q4	
Q5	
Total	

Default technology:

- 22nm Low Standby Power Process (LSTP)
- $\gamma = 1$
- V_{dd}=800mV
- nominal $V_{thn} = -V_{thp}$=300mV
- $C_0 = 2 \times 10^{-17}$F (for $W = 1$ device)
- $I_{d,sat_0} = 10\mu$A (for $W = 1$ device)
- $I_{sd,leak_0} = 0.3$ pA (for $W = 1$ device)
- velocity saturated operation
- $R_{wire} = 700\text{K}\Omega/\text{cm}$
- $C_{wire} = 1.7\text{pF}/\text{cm}$

Device	V_{gs}	I_{ds}
NMOS	$V_{gs} < V_{thn}$	$(1 \times 10^{-6})\, W e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$2 \times 10^{-5} W\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(-1 \times 10^{-6})\, W e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$2 \times 10^{-5} W\,(V_{gs} - V_{thp})$

Timing constraints:

$$T \geq t_{clk \to q} + t_{plogic} + t_{setup} \tag{1}$$

$$t_{cdlatch} + t_{cdlogic} \geq t_{hold} \tag{2}$$

Optimal buffering:

$$L_{seg} = 2\sqrt{\frac{R_0(\gamma+1)C_0}{R_{wire}C_{wire}}} \tag{3}$$

$$W_{buf} = \sqrt{\frac{R_0 C_{wire}}{2R_{wire}C_0}} \tag{4}$$

1. (20pts) Speed and Power. Consider using CMOS nand2 gates minimum sized in the default technology. Specify units in all answers.

   (a) Assume the default technology and calculate $\tau = R_0 C_0$.

τ	

   (b) Assume the critical path in the design (including flip-flop setup time and clock-to-q delay) can be modeled as a series chain of 10 of these gates, each loaded by 4 equivalent gates. What is the maximum frequency of operation possible?

Max Frequency	

   (c) Assuming chip cooling allows a maximum dynamic power dissipation of 1W (leakage is negligible), when operating at the frequency from part (b), what is the maximum number of gates that can switch during a clock cycle, on average?

Max gate-evals/clock	

   (d) Assuming the output of one of these gates drives a single gate input through an unbuffered wire with $R_{wire} = 700\text{K}\Omega/\text{cm}$, $C_{wire} = 1.7\text{pF/cm}$, what is the maximum distance the signal can travel in one clock cycle at the maximum clock frequency identified (part b)?

Max Distance	

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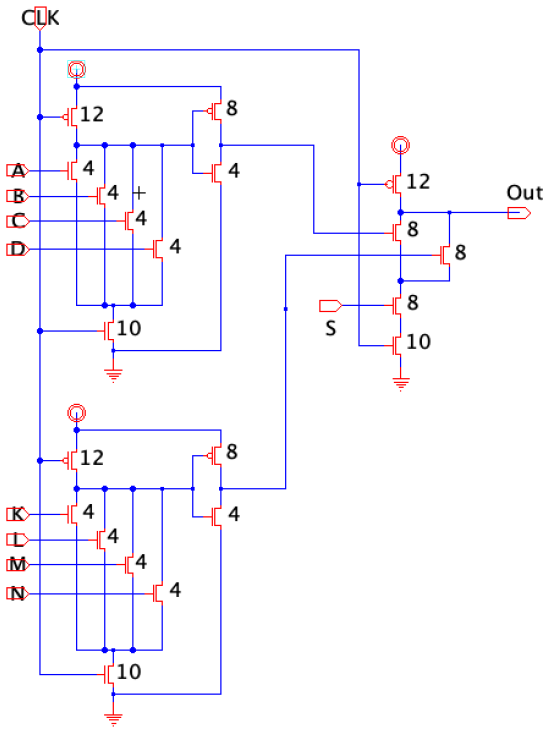
2. (20pts) Consider the following dynamic logic circuit. What logic function does it evaluate?

   Assume the circuit is loaded by $7C_0$ output. Assume $C_{diff} = 0.5C_{gate}$, $\mu_n = 2\mu_p$. Assume the CLK signal is driven strongly such that the rise time on the clock is R_0C_0. Use Elmore delay calculations where appropriate. For full credit (and partial credit consideration) show your delay components (stages, components of Elmore delay calculation).



Out as a function of the inputs?	
Evaluate Delay in units of τ (show delay components)	
Precharge Time	

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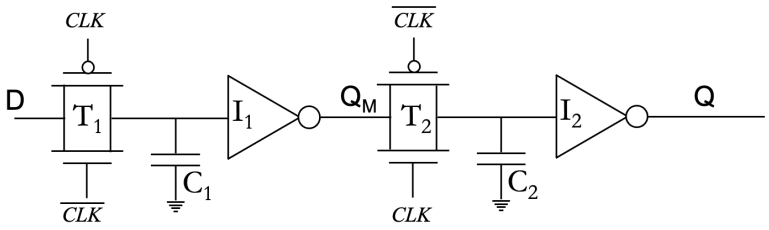
3. (20pts) Below is a register built from cascading two dynamic latches. C_1 and C_2 are not explicit capacitors but just from the parasitics at each node. Assume the clocks are ideal non-overlapping clocks with a frequency of 250MHz. Each transmission gate has a delay of 100ps and each inverter has a delay of 200ps.



(a) Is this a positive or negative edge-triggered device?

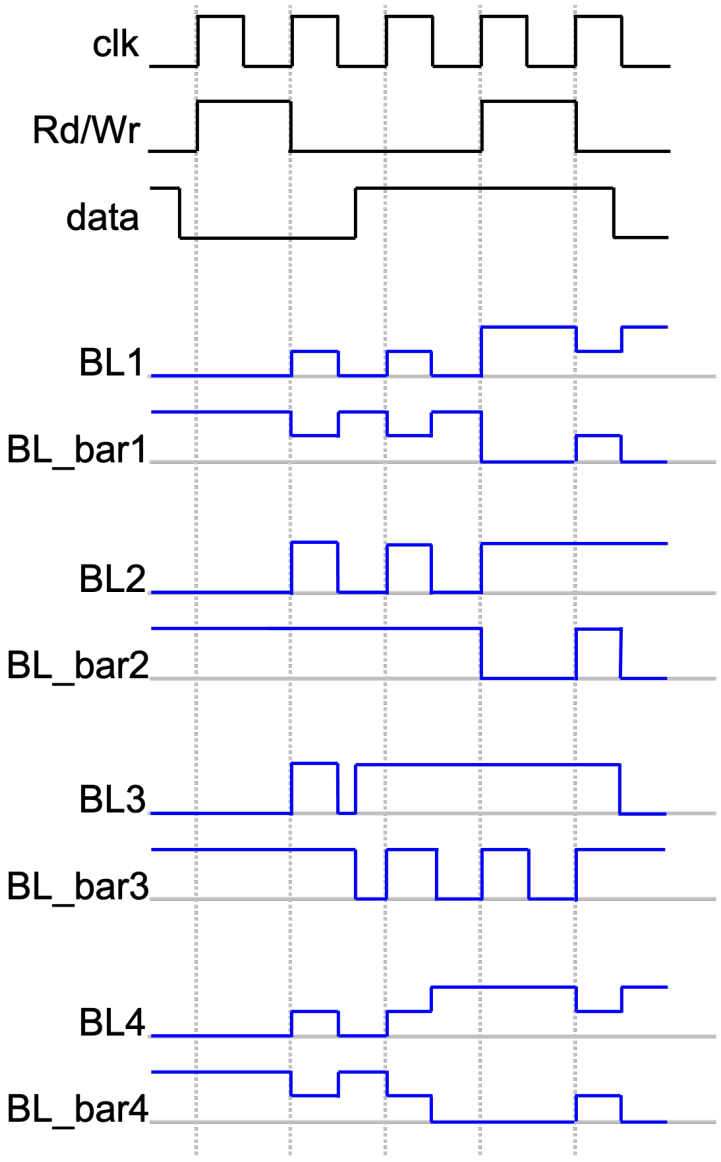
(b) determine the register timing parameters. Include units.

i. Setup time

ii. Hold time

iii. Worst case clock-to-q delay

4. SRAM (20 points). 4 different 6T SRAM cells are designed and tested for correct operation. There are three input test signals: clk, $\overline{\text{Rd}}$/Wr, and data. A single read or write operation occurs in a single clock period. When $\overline{\text{Rd}}$/Wr is high a write operation should occur, and when it is low a read operation should occur. The data signal gives what data should be written into the cell when doing a write operation. Below are the test signals and BL and BL bar of all 4 cells. For each cell, indicate whether the cell is exhibiting correct operation. If not, explain what is not correct about the operation. Answer table on next page.



Bitcell 1	
Bitcell 2	
Bitcell 3	
Bitcell 4	

5. (20pts) Short Answer Questions: Answer the questions briefly. Include diagrams and equations as needed. Be **clear** in your explanation and **handwriting**.

   A Identify and describe two differences between SRAM and DRAM memory cells.

   B What is a sense amplifier and why might you need it?

   C What is a memory read upset and what is one way you can avoid them?

   D Draw a schematic of a tristate buffer and draw its truth table.