Course Webpage

Circuit-Level Modeling, Design, and Optimization for Digital Systems

Course: ESE3700

Units: 1.0 CU
Term: Spring 2025
When: MW 1:45pm-3:14pm EST (all times below are EST)
Where: Towne 307
Instructor: Jing (Jane) Li (Levine 274, seas: janeli)
Instructor Office Hours: W 3:15pm - 4:15pm
Head TA: Peter Proenca (seas: peterpro) (office hours: TBA)
TA: Tim Liang (seas: tliang3) (office hours: TBA)
TA: Kiet (Keith) Cao (seas: kietc) (office hours: TBA)

Prerequisites: ESE 150, ESE 215, CIS 240 is also highly recommended. Roundup of topics you should be familiar with.
URL: `<http://www.seas.upenn.edu/~ese3700/>`

Quick Links: [Course Objectives] [Grading] [Policies] [Spring 2025 Calendar] [Reading] [Student Advice] [Tool Guides]

Catalog Level Description: Circuit-level design and modeling of gates, storage, and interconnect. Emphasis on understanding physical aspects which drive energy, delay, area, and noise in digital circuits. Impact of physical effects on design and achievable performance.

https://www.seas.upenn.edu/~ese3700/

ESE3700: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 1: January 15, 2025

Introduction and Overview

Course Structure: Staff

- Course Staff (complete info on course website)
- Instructor: Jing (Jane) Li (she/her)
  - OH: W 3:15pm-4:15pm, Levin 274
  - Email: janeli@seas.upenn.edu
    - Best way to reach me
- Website:
  - https://li.seas.upenn.edu/
  - https://cybersavvy.seas.upenn.edu/

Head TA: Peter Proenca

- About me:
  - Took ESE 3700 in Spring 2023
  - Senior studying CMPE
  - Accelerated Masters – ESE
  - I am interested in medicine and the combination of engineering and health.
  - Outside of engineering I play a variety of instruments and I like to swim.
- Email: peterpro@seas.upenn.edu

TA Introduction: Tim Liang

- Took ESE 3700 in Spring 2024 (One of my favorite courses)
- Junior in CMPE
- Outside of class, I enjoy exploring the outdoors and gaming
- Happy to chat about the CMPE major, hobbies, or anything else
- Email: tliang3@seas.upenn.edu

TA Introduction: Kiet (Keith) Cao

- Took ESE 5700 in Fall 2024
- First year EE master student; Undergraduate from Cornell
- I worked as R&D engineer in IoT sector before joining UPenn
- I like basketball, badminton, running, cooking, and happy to chat about work/hobby/etc
- Email: kietc@seas.upenn.edu

What I do for research?

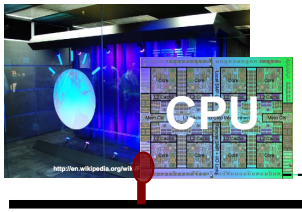
50W

~10^5 Gap

2MW

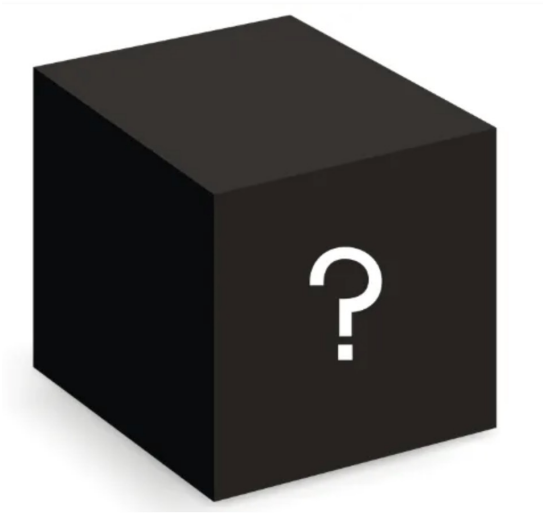
90 IBM 750 severs

- **2880 P7 cores**
- **16TB RAM**



What I do for research?

Treat Computer as a Blackbox



SW/HW Co-Design

What I do for research? –Workload Optimized Systems

Search

Penn Today

Penn Engineering's ENIAD sets new world record for energy–efficient supercomputing

ENIAD, named after ENIAC, the world's first digital computer, which was developed at Penn 75 years ago, took the top spot among a list of 500 of the most energy–efficient supercomputers reported in the world.

Evan Lerner · August 10, 2021

https://penntoday.upenn.edu/news/penn-engineerings-eniad-sets-new-world-record-energy-efficient-supercomputing

What I do for research? (a vision on memory)

https://www.youtube.com/watch?time_continue=3&v=67VKORQX4T4&feature=emb_logo

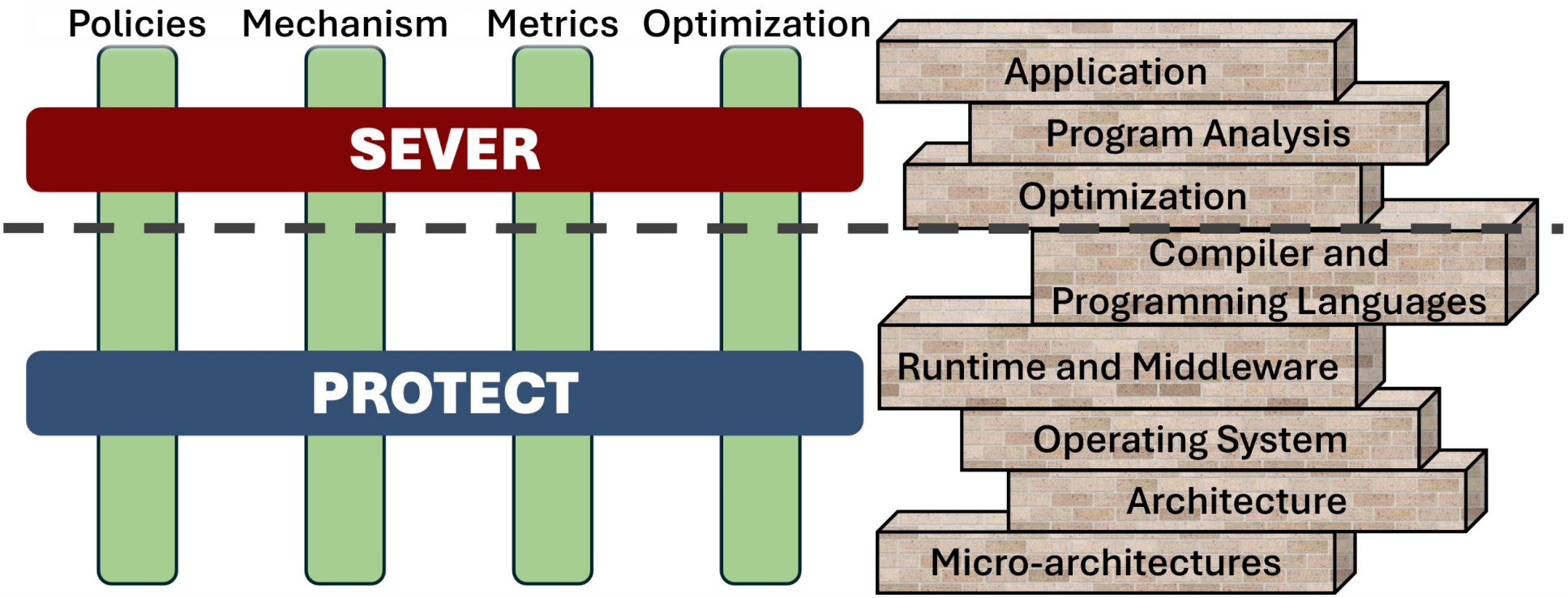
What I do for research?

CyberSavvy Center

https://cybersavvy.seas.upenn.edu/

What I do for research?

CyberSavvy Center



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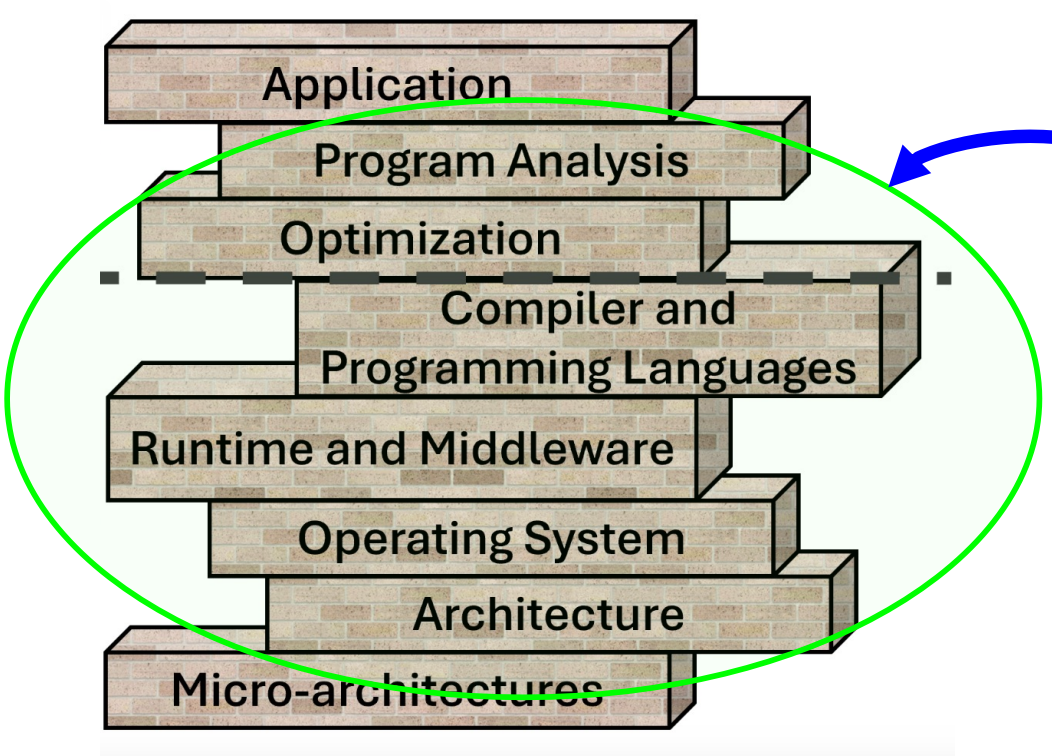
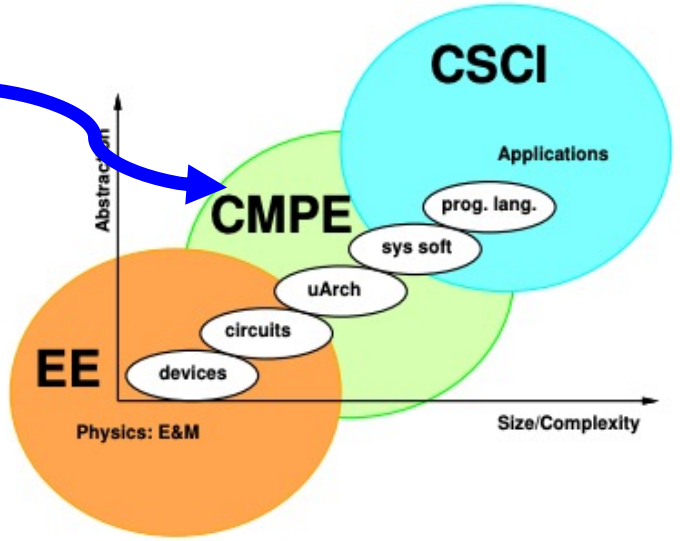
What I do for research?

CyberSavvy Center





https://cmpe.seas.upenn.edu/wp-content/uploads/2018/07/CMPE-Major-Description_ESE_19.pdf

https://cybersavvy.seas.upenn.edu/

What I do for research/teaching?

AI/Machine Learning

ESE 5390

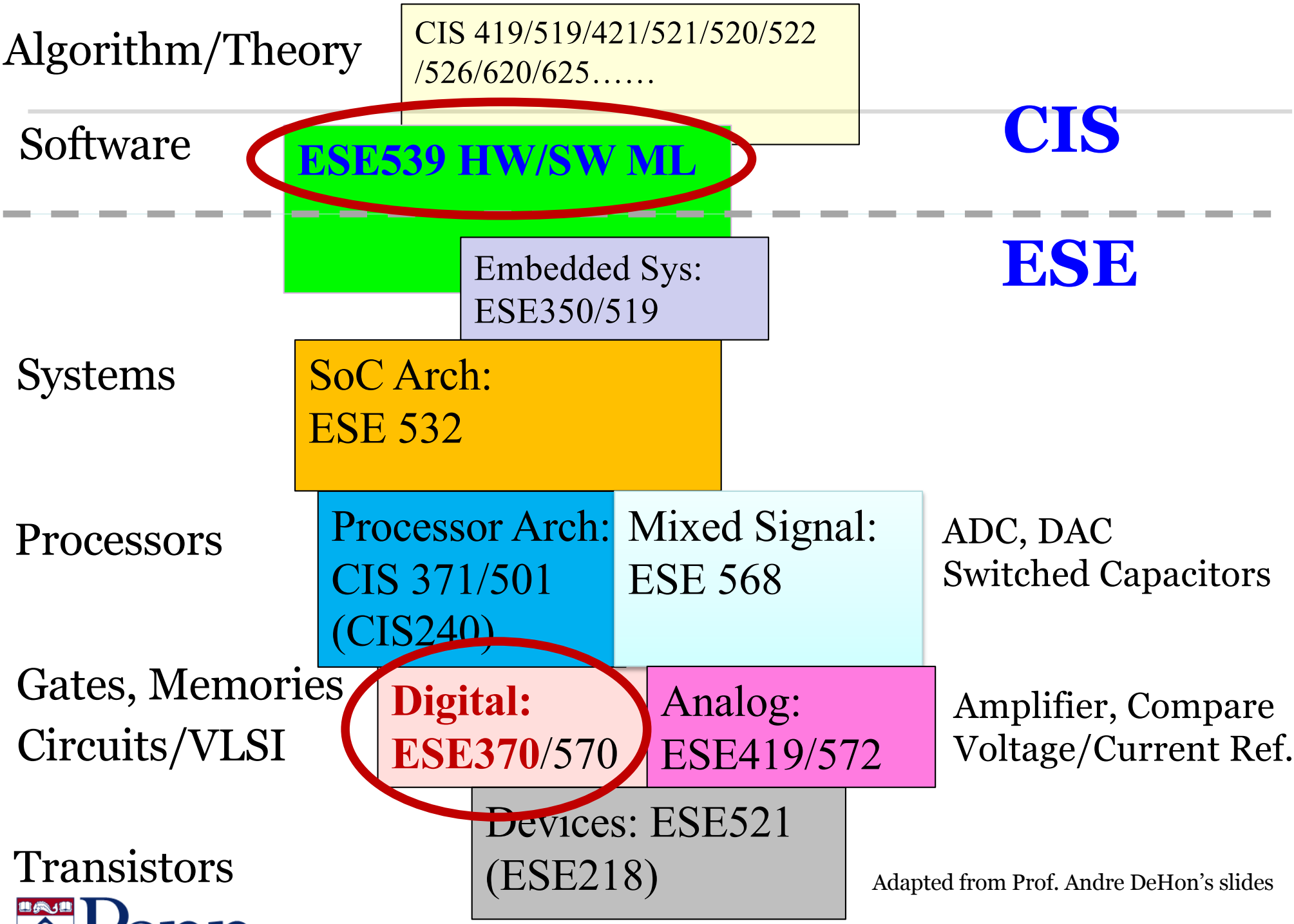
SW/HW Co-Design for Machine Learning

Computer System

SysML: The New Frontier of Machine Learning Systems

Alexander Ratner, Dan Alistarh, Gustavo Alonso, Peter Bailis, Sarah Bird, Nicholas Carlini, Bryan Catanzaro, Eric Chung, Bill Dally, Jeff Dean, Inderjit S. Dhillon, Alexandros Dimakis, Pradeep Dubey, Charles Elkan, Grigori Fursin, Gregory R. Ganger, Lise Getoor, Phillip B. Gibbons, Garth A. Gibson, Joseph E. Gonzalez, Justin Gottschlich, Song Han, Kim Hazelwood, Furong Huang, Martin Jaggi, Kevin Jamieson, Michael I. Jordan, Gauri Joshi, Rania Khalaf, Jason Knight, Jakub Konečný, Tim Kraska, Arun Kumar, Anastasios Kyrillidis, Jing Li, Samuel Madden, H. Brendan McMahan, Erik Meijer, Ioannis Mitliagkas, Rajat Monga, Derek Murray, Dimitris Papailiopoulos, Gennady Pekhimenko, Theodoros Rekatsinas, Afshin Rostamizadeh, Christopher Ré, Christopher De Sa, Hanie Sedghi, Siddhartha Sen, Virginia Smith, Alex Smola, Dawn Song, Evan Sparks, Ion Stoica, Vivienne Sze, Madeleine Udell, Joaquin Vanschoren, Shivaram Venkataraman, Rashmi Vinayak, Markus Weimer, Andrew Gordon Wilson, Eric Xing, Matei Zaharia, Ce Zhang, Ameet Talwalkar

White Paper: https://arxiv.org/abs/1904.03257



Adapted from Prof. Andre DeHon's slides

CMPE FEEDBACK SESSION

Wed, January 15th

3:30-4:30pm
Raisler Lounge (Towne 225)
Snacks available

Lecture Outline

- Course Overview
  - Motivating questions
  - What this course is about
  - Learning objectives
  - What you need to know
- Course Details
  - Course structure
  - Course policies
  - Course content

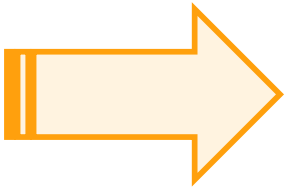
Virtually all apps will become AI centric

Ion Stoica, SIGMOD'20

Ubiquitous Supercomputer: Smaller Scale, Heavily Integrated

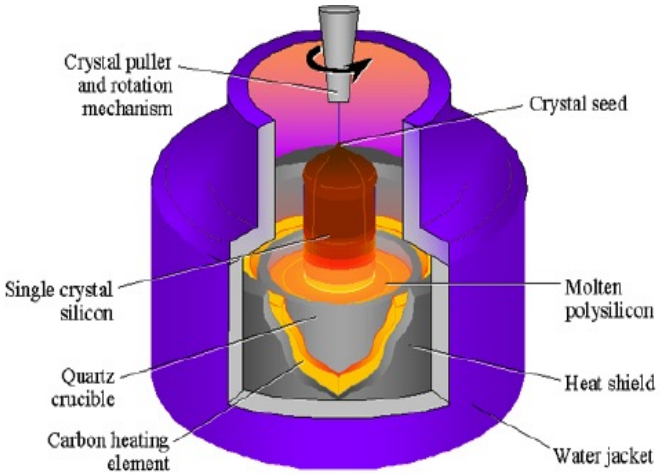
Cray 2, 1985	iPhone 4, 2010	Apple Watch, 2015	**~ 2B FLOPs**
CM-5, 1991	2x Samsung S6	1 Haswell Core	**~100B FLOPs**
IBM ASCI Red, 2000	Playstation 4, 2013	32-core Haswell	**~3,000B FLOPs**

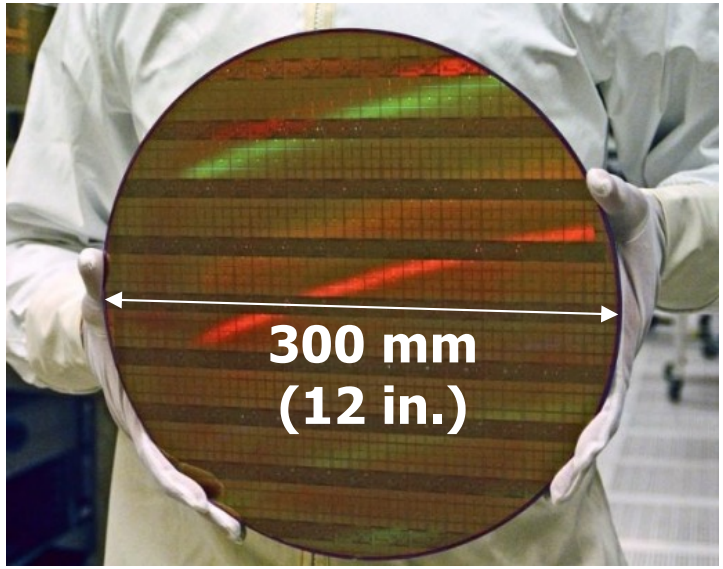
https://pages.experts-exchange.com/processing-power-compared

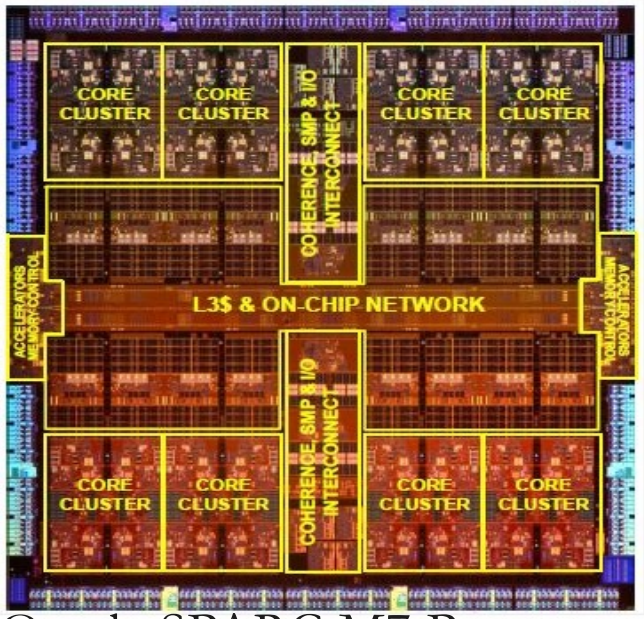


https://www.datacenterknowledge.com/supercomputers/

VLSI Design



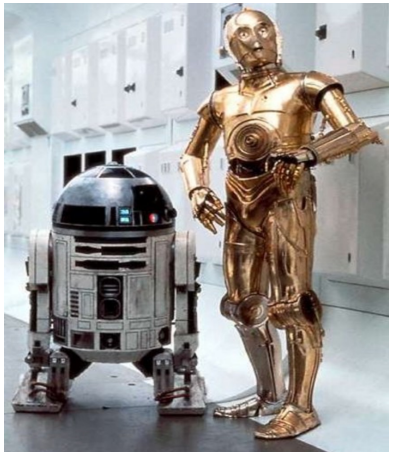




Oracle SPARC M7 Processor

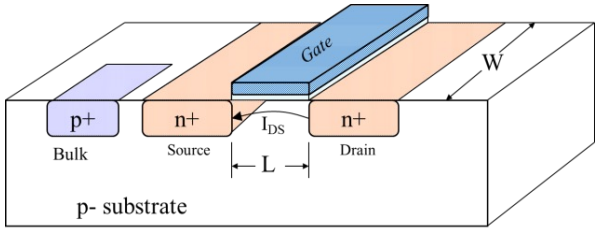
What this course about?

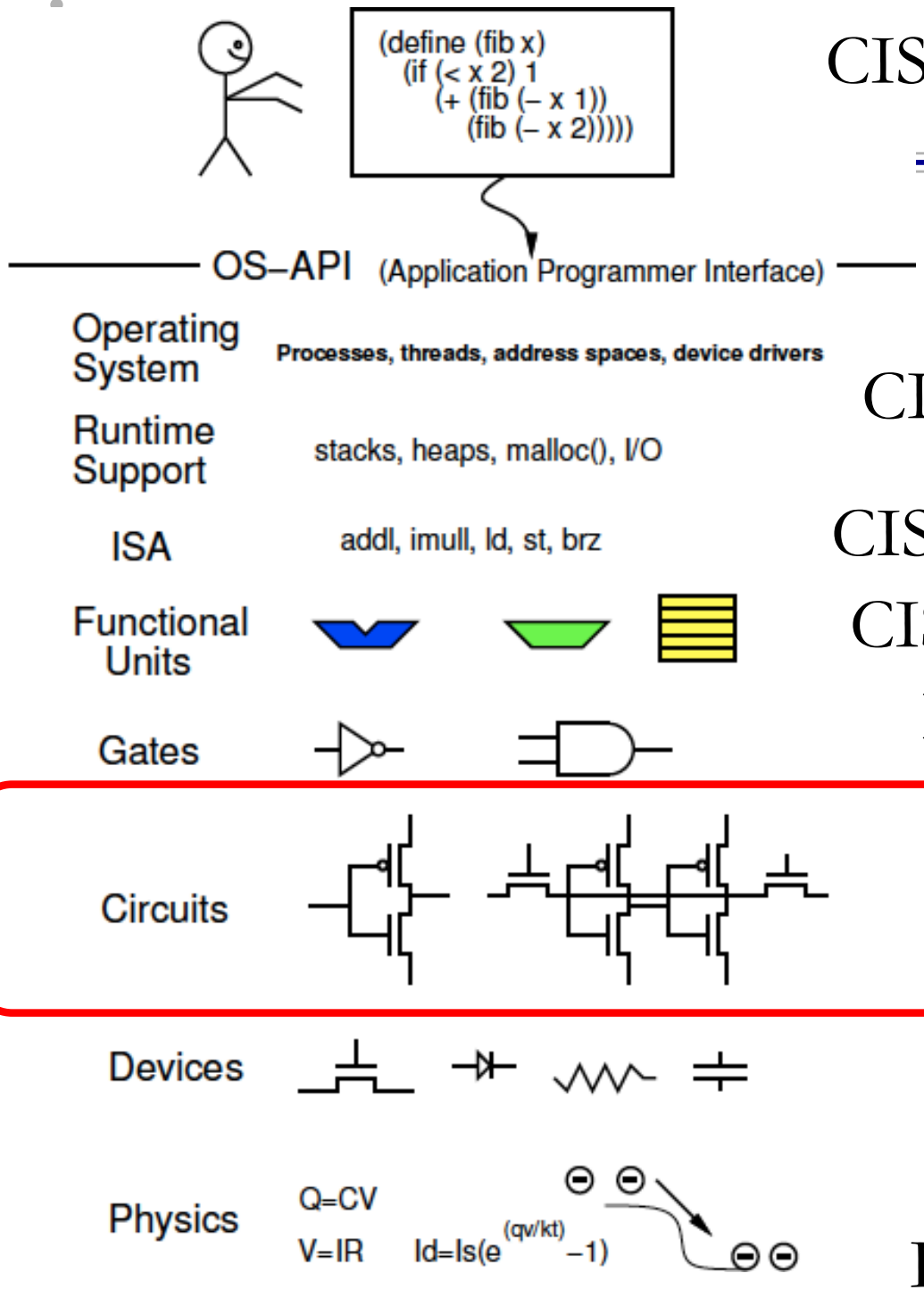
To build something you have to understand what building blocks you have available to you.



To build something really cool you need to have a fairly intimate understanding of how those building blocks work.

In VLSI our two primary building blocks are the NMOS and PMOS transistors. This is not a device physics course, but we will have to dive a bit into the workings of these transistors.





CIS120/121

CIS380

CIS240

CIS371, ESE532, ESE539

ESE150

We are here.

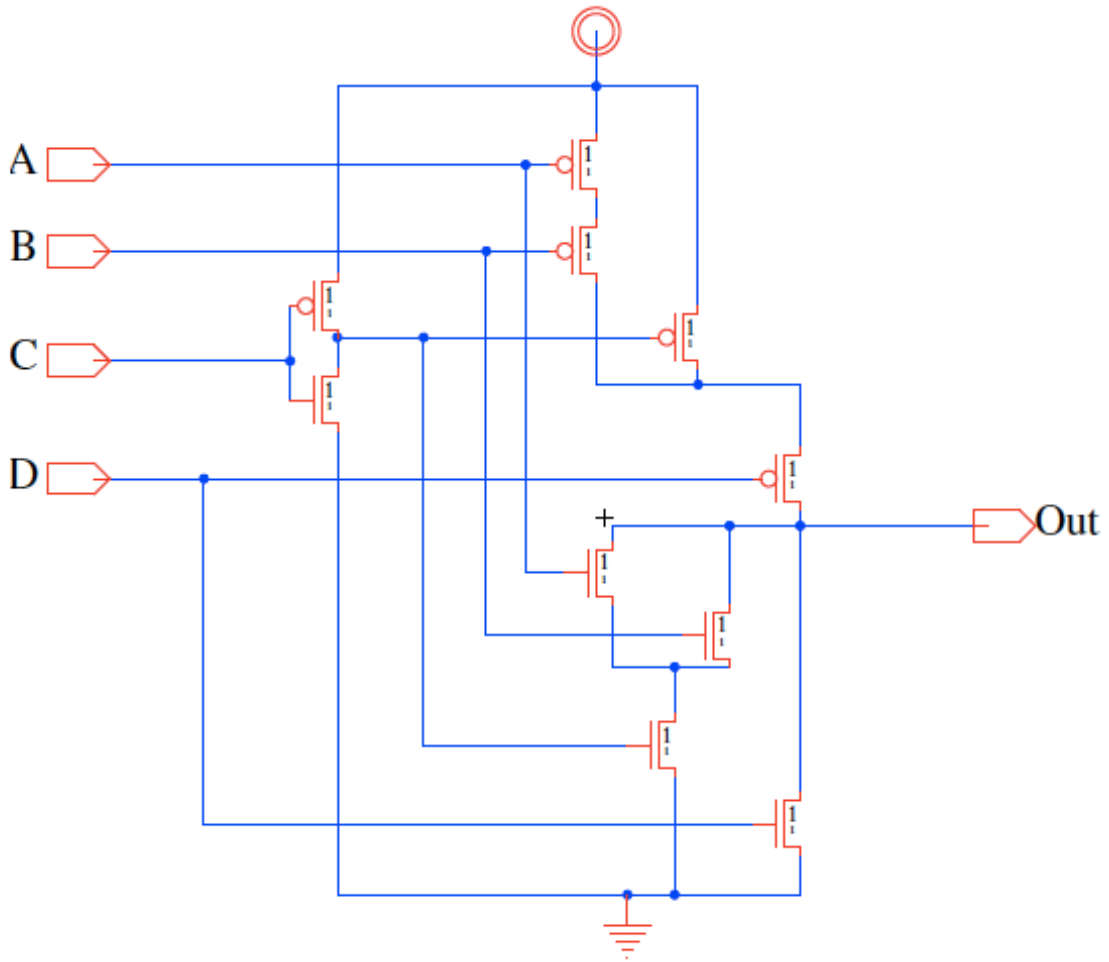
ESE215, ESE319

ESE218

ESE112/Phys151

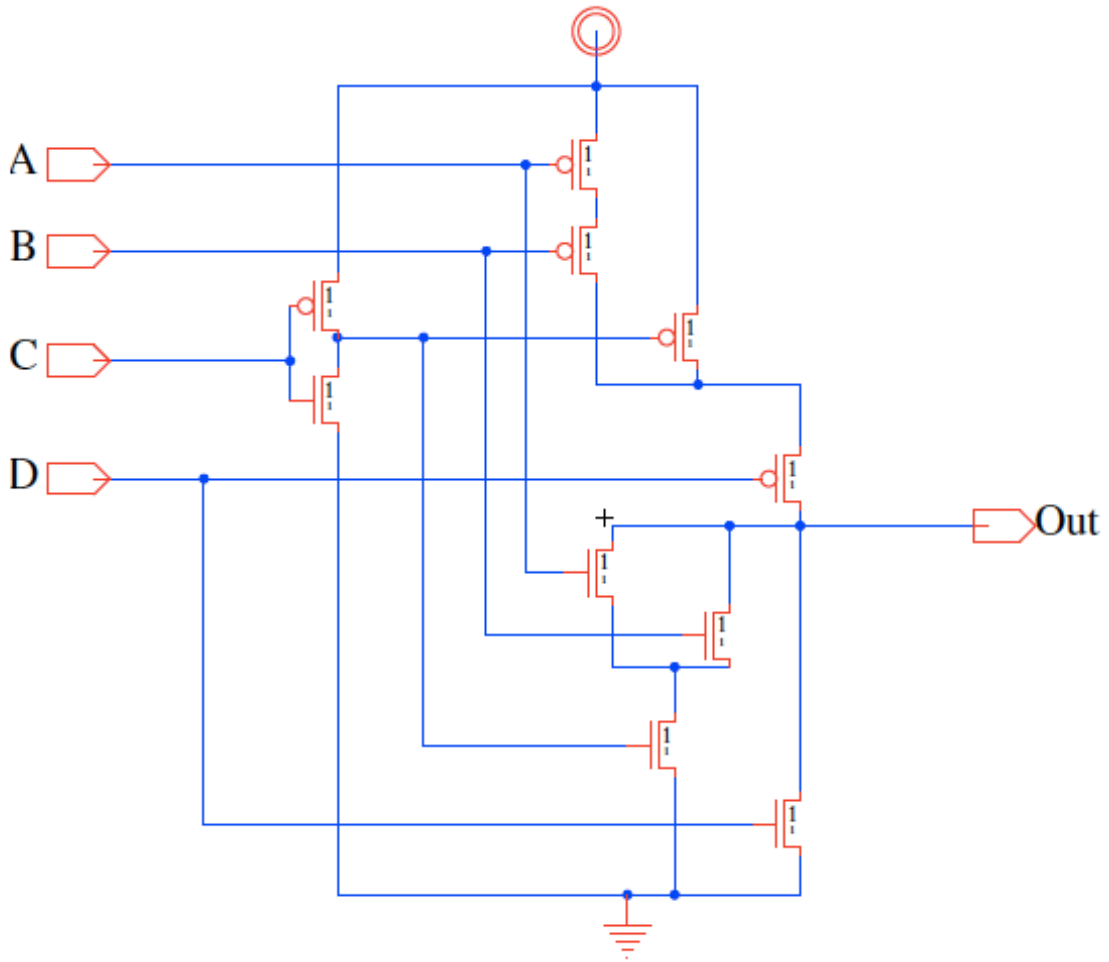
Sample Problems

- What does this circuit do?



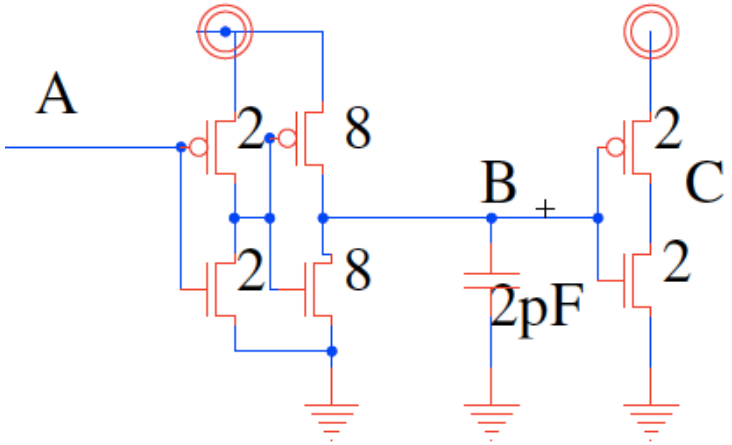
Sample Problems

- What does this circuit do? How fast does it operate?



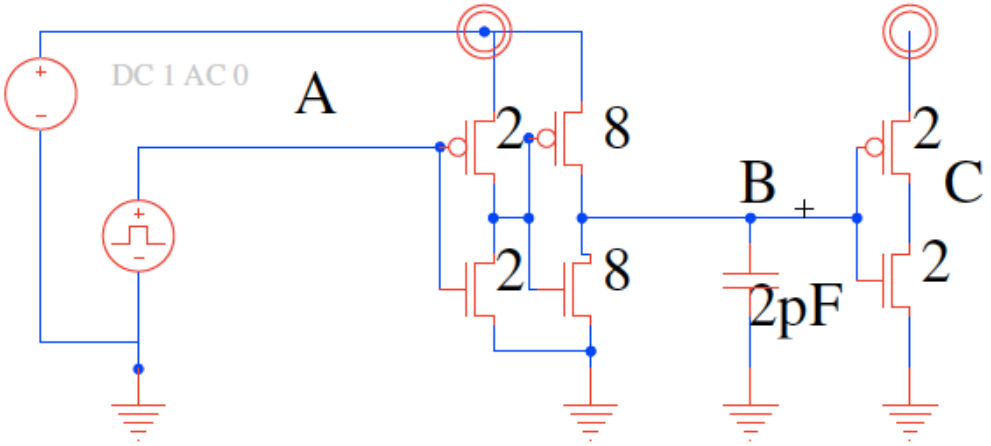
Sample Problems (con't)

- What does this circuit do? How are A, B, C related?



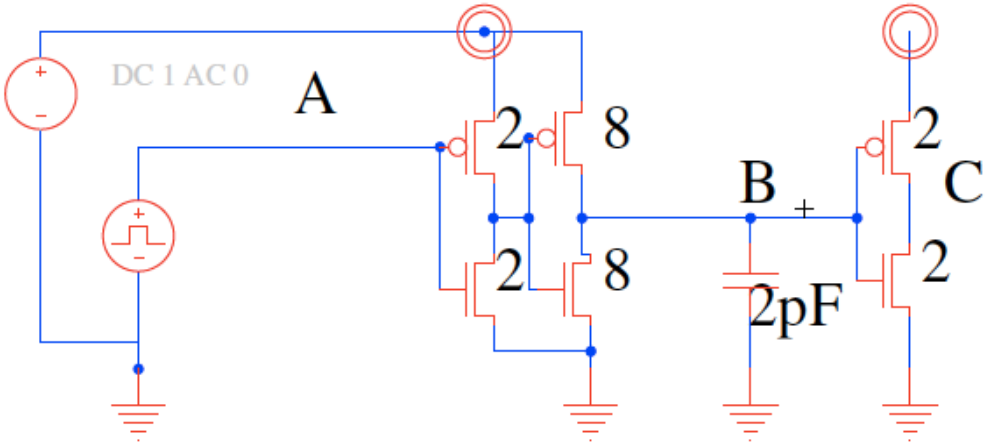
Sample Problems (con't)

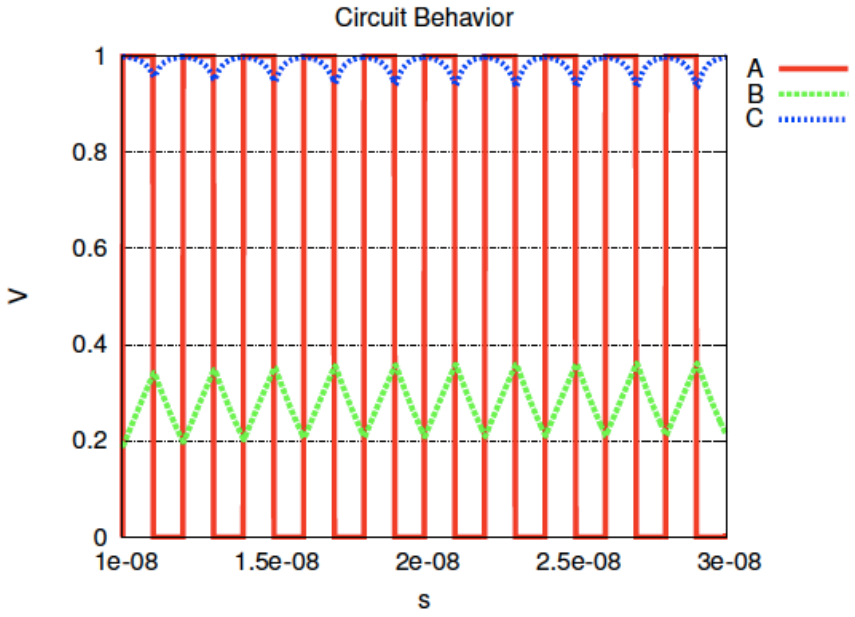
- What does this circuit do? How are A, B, C related?



Sample Problems (con't)

- What's wrong here? How do we fix it?





Limits?

- Consider a 22nm technology
- Typical gate with W=3, 2-input NOR
- Use chip in cell phone
- What prevents us from running 1 billion transistor chip at 10GHz?

Impact of Voltage?

- If we have a chip running at 1GHz with a 1V power supply dissipating 1W.
- What happens to performance if we cut the power supply to 500mV?
  - Speed?
  - Power?

What this course is about

- Modeling and abstraction
  - Predict circuit behavior
  - …well enough to know your design will work
  - …with given performance spec(ification)s
    - Speed, energy, size, etc.
  - …well enough to reason about design and optimization
    - What knob can I turn to make faster?
    - How much faster can I expect to make it?

What this course is about (con't)

- Modeling and abstraction
  - Back-of-the-envelope calculations
    - Simple enough to reason about and estimate
      - …without a calculator
  - Sensitive to phenomena
    - Able to think through the details
  - With computer assistance
    - …understanding even that is a simplified approximation of phenomenology

Learning Objectives

- Disciplines for robust digital logic and signaling
  - (*e.g.*, regeneration, clocking)
- Where delay, energy, area, and noise arise in gates, memory, and interconnect
- Modeling these physical effects
  - back-of-the-envelope design
    - (*e.g.* RC and Elmore delay)
  - detailed simulation

Learning Objectives (con't)

- Tradeoffs in performance specs
  - Among delay, energy, area, noise
- How to design and optimize
  - logic, memory, and interconnect structures
  - at the gate, transistor, and wire level
- How technology scales
  - impact on digital circuits and computer systems

What you need to know

- See "knowledge roundup" topics page linked from course webpage
- ESE 150 (CIS 240)
  - Gates, Boolean logic, DeMorgan's, gate optimization, K-maps
  - Review: book chapter in Canvas
- ESE 215
  - RLC circuit analysis
  - Review: 215 lectures posted in Canvas
- Diagnostic Quiz on Canvas
  - Not graded, weighted as a homework assignment
  - Complete by Friday 1/24 midnight
  - 150 and 215 review materials in Canvas Files section

Course Structure: Websites

- Website (http://www.seas.upenn.edu/~ese3700/)
  - Course calendar is used for all handouts (preclass, lecture slides, assignments, and readings)
  - Canvas used for assignment submission, grades
  - Ed Discussion used for announcements and discussions

Course Structure: Lectures

- MW 1:45pm-3:14pm Lecture in Towne 307
- Preclass and lecture slides posted online before class
- Readings from textbook
- 2 lecture periods → Labs in Detkin

ESE3700 Spring 2025 Working Schedule

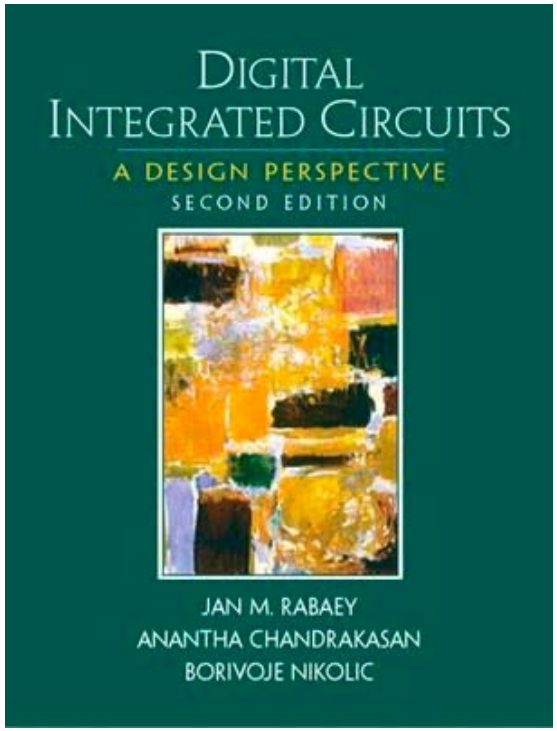
Wk	Lect.	Date		Lecture	Slides	Due	Reading
1	1	1/11	W	Intro/Overview	[lec1] [lec1_6up]		1 through 1.2; review course web page completely
2		1/16	M	MLK Jr. Day (no class)			
	2	1/18	W	Transistor Introduction (basics) and Gates from Transistors	[lec2_pc] [lec2] [lec2_6up]		review ESE215; 6.2 through static properties in 6.2.1
		1/20	F			Diagnostics Quiz (canvas)	
		1/23	M	Lab 1 (Detkin): Gate from Discrete Transistors			[Lab Instructions]

Course Structure: Lectures (Physical)

- **Delivered in person (Mask recommended)**
- Statistically and empirically speaking, you will do better if you come to lecture
- Better if interactive, **everyone** engaged
  - Asking and answering questions
  - Actively thinking about material every day
  - Gain **participation credit!!**
- Two things
  - **Preclass worksheet exercises**
    - Primes you for topic of the day
    - Will be addressed during lecture
    - **Important for exams!!**
  - Ask questions of individuals

Course Structure: Textbook

- Textbook
  - *Digital Integrated Circuits, A Design Perspective*, Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, 2nd edition
    - Great reference text with great detail
    - REALLY!! useful for projects



Course Structure: Assignments/Exams

- Homework – (mostly) week long (6 total) [3%*6=18%]
  - Due F at midnight
  - Submit in Canvas
- Projects – 3 weeks long (2 total) [15% +20%]
  - Design/Simulation oriented
  - 20% *max (proj 1, proj 2) +15% *min (proj 1, proj 2)
  - On two main topics
    - 1: Computation - Solo
    - 2: Memory – Team of 2
- Midterms [15% and 22%] (2 total)
  - 22% *max (mid 1, mid 2) +15% *min (mid 1, mid 2)
- Participation [10%]

Course Structure: Admin

- Use course calendar
  - Lectures and preclass online before class
    - Will post night before class
    - Reserve the right to change them (usually minor)
  - Homework/projects linked
    - Homework 1 out now
  - Reading for whole term specified
- Take notes!
  - Especially on the preclass examples we do in class
  - Slides have a lot of questions – not a lot of answers

Course Policies

See course web page for full details

- Turn assignments in on Canvas
  - Anything handwritten/drawn must be clearly legible
    - No handwritten work allowed on projects
  - Submit CAD generated figures, graphs, results when specified
  - Late Policy – allowed **5 late days** for whole semester
    - Can only use a max of three days on each project
    - Allowed late days (D) for group projects
      - If max (Student 1, Student 2) ≤ 3, D= max (Student 1, Student 2)
      - If max (Student 1, Student 2) > 3, D=3
- Individual work (HW & Project)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help

Course Content

- Logic (Computation) [11 weeks]
  - Combinational logic
  - Sequential logic
- Memory/Storage [4 weeks]

Course Content (con't)

- Logic
  - Transistors → Gates
  - **Lab:** build gate, measure delay
  - Regeneration (noise margins)
  - Delay
  - Area (no layout → ESE370)
  - Energy
  - Synchronous (flip-flops, clocking, dynamic)
  - **Project 1:** fast ripple-carry adder

Course Content (con't)

- Memory/Storage
  - No Lab component
  - RAM Organization
    - Memory cells and periphery circuits
  - Driving Large Capacitances
  - Signal amplification/regeneration
  - Noise: Crosstalk
  - **Project 2:** design a SRAM

Absence

- Excused absences are only granted in cases of medical issues, family emergencies or other concerns that necessitate missing class
- Excused 'other concerns' are determined case-by-case based on urgency, necessity and gravity of the concern
- Regardless if excused or not, absences must be documented by using Path@Penn

Ed Discussion Posting Policy

- All posts must be in accordance with the collaboration policy
- No images of text (such as logs) are allowed
- Duplicate questions will not be answered
- Posts about labs and projects must include a *good faith* attempt at the answer
  - What have you tried so far?
- Exact values of your results should not be posted (use orders of magnitude)
- Posts against these rules will not be answered or will be removed
- If in doubt, post privately to instructor and TAs

Post-Covid Masking Policy

- Masks are recommended in lecture or office hours for everyone's safety and peace of mind

Advice

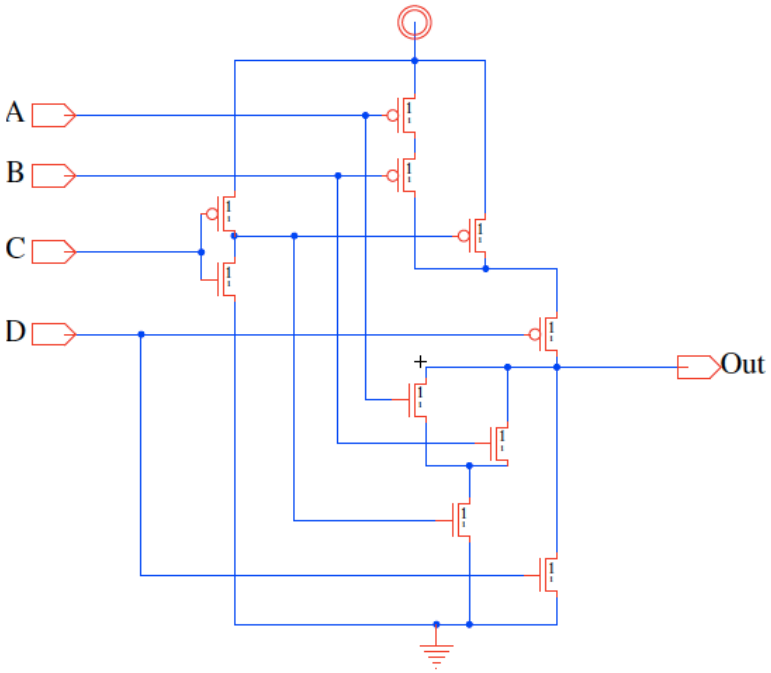
- Course is hard (but valuable)
- Should be thinking about this material every day
- Go to office hours
- MUST READ TEXT! DO **PRECLASS!**
- Learning is spread over all components
  - Lecture, reading, **homework, projects**, exams
- Cannot pass the class if you don't turn in projects
  - Give yourself enough time. They will take you longer than you think

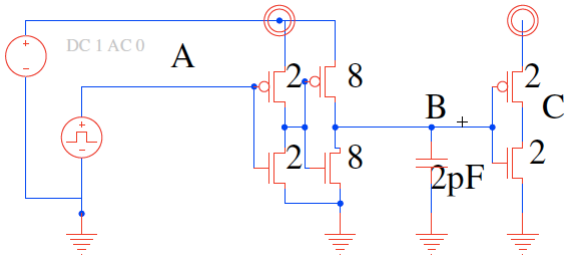
Advice from your fellow students:

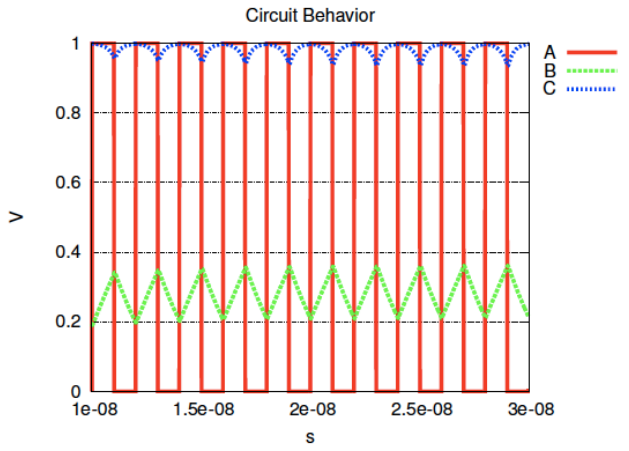
- Q: As a current or former student that did very well in ESE 370, what advice do you have for future students to be successful in ESE 370?
  - "The most important thing for me was to **attend lecture**"
  - "make sure you **start early** on the projects"
  - "ESE 370 is a class that **moves quickly**… best ways to stay abreast of the material was to engage with it … **ask questions and engage** in conversation in class (or in office hours) regularly"
  - "ESE 370 is a very **rewarding class, but not an easy class**. The biggest advice I can offer is to **stay on top of the work**."
  - "will be both very **challenging and rewarding**, and quite **unique compared to other classes at Penn**"
- See course webpage for full answers

Big Ideas

- Model (a.k.a. analysis and simulation) to enable real-life robust IC design and optimization







Admin

- Find web, get text, assigned reading…
  - http://www.seas.upenn.edu/~ese3700
  - https://canvas.upenn.edu/courses/
- To do:
  - Check your access to Canvas and Ed Discussion
  - Diagnostic Quiz (in Canvas) – due by F 1/24
    - Review as needed
  - HW 1 out now – due F 1/31
    - Need lab and future lectures to finish

CMPE FEEDBACK SESSION

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Acknowledgement

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- Prof. Tania Khanna (University of Pennsylvania)