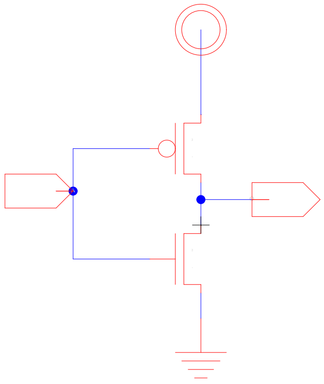
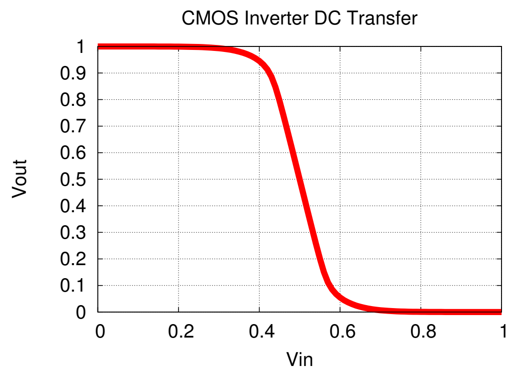
Device	V_{gs}	I_d
NMOS	$V_{gs} < V_{thn}$	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$-1.8 \times 10^{-4}\,(V_{gs} - V_{thp})$

Consider an inverter using the pmos and nmos devices described above:





Useful: $e^{-1} \approx 0.37$, $e^{-4} \approx 0.02$, $e^{-7.5} \approx 6 \times 10^{-4}$,

1. V_{dd}=1V, V_{thn}=300mV, V_{thp}=-300mV, assume the static current is in steady-state operation and dynamic/short circuit current are the peak currents at V_{in} given.

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}	
0V				A
140mV				B
400mV				C
500mV				D
600mV				E
860mV				F
1V				G

2. V_{dd}=520mV, V_{thn}=300mV, V_{thp}=-300mV, assume gate is unloaded (no output capacitance to charge).

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}	
0V				A, F
140mV				B, G
260mV				C
380mV				D
520mV				E

3. V_{thn}=300mV, V_{thp}=-300mV, V_{in}=V_{dd}; estimate $\tau = CV/I$

V_{dd}	I_{dyn}	$\frac{\tau}{\tau(V_{dd}=1V)}$	$\frac{E_{switch}}{E_{switch}(V_{dd}=1V)}$	$E\tau$	
1V		1	1	1	all
700mV					A, E
500mV					B, F
350mV					C, G
260mV					D

4. V_{dd}=1V, V_{in}=V_{dd}

V_{thn} = -V_{thp}	I_{dyn}	$\frac{\tau}{\tau(\lvert V_{th}\rvert=300mV)}$	I_{static}	$\frac{I_{static}}{I_{static}(\lvert V_{th}\rvert=300mV)}$	
300mV		1		1	all
460mV					A, B, C
600mV					D, E, F, G

Device	V_{gs}	I_d
NMOS	$V_{gs} < V_{thn}$	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$-1.8 \times 10^{-4}\,(V_{gs} - V_{thp})$