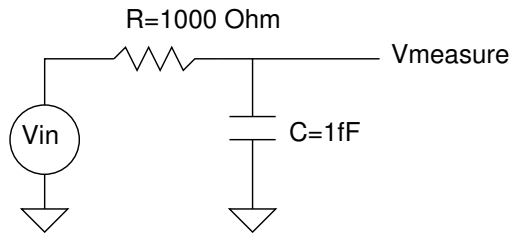


Assume  $V_{in}$  is 0 for  $t < 0$  and steps to 1V at  $t = 0$ .

1. What value does  $V_{measure}$  take on as  $t \rightarrow \infty$  ?


2. Assume  $V_{in}$  is 0 for  $t < 0$  and steps to 1V at  $t = 0$ . The circuit is then allowed to achieve steady-state.

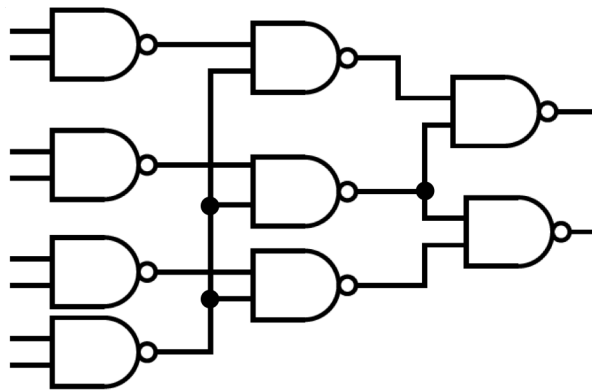


- (a) What is the time constant,  $\tau$ ?
- (b) How many seconds does it take before  $V_{measure}$  reaches 90% of the final value? Use the table below and  $e = 2.72$ .

t (in ps)	$e^{-t/\tau}$	$1-e^{-t/\tau}$
0		
0.1		
1		
2		
2.3		

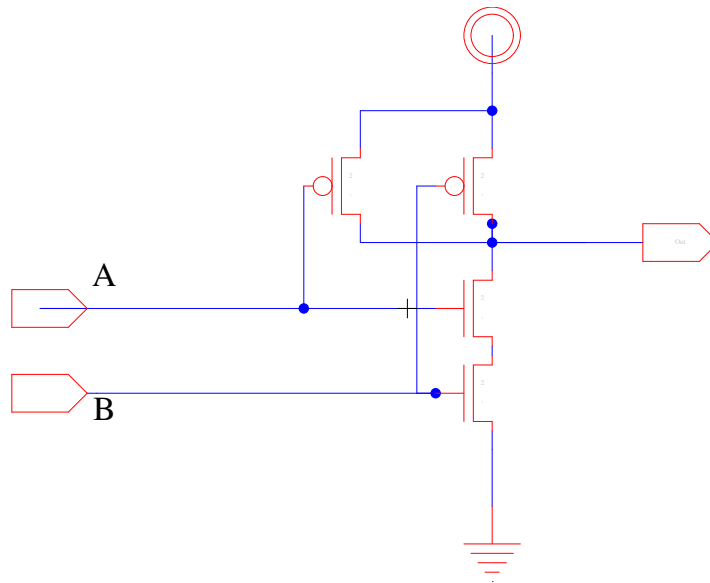
- (c) At what time does  $V_{measure}$  reach 50% of its value? Use  $\ln(0.5) = -0.69$ .

3. Assume each gate puts a load of 1 on each of its two inputs. (All intersecting wires are **not** connected)



What is the load on the most heavily loaded gate output?	
What is the load on the least heavily loaded gate output?	

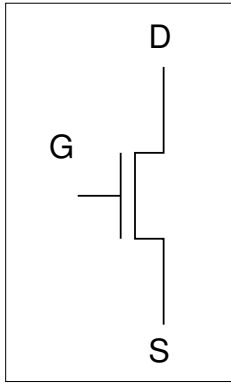
4. Assuming  $R_{on,p}=R_{on,n}=R_{on}$ , what are all the possible equivalent resistance values of the gate output stage?



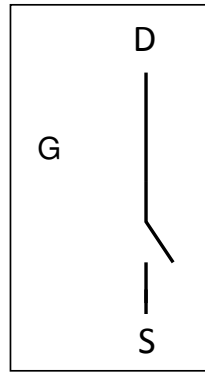
**Hint:** How many cases are there? What is the resistance for each of the cases?

Case	Resistance

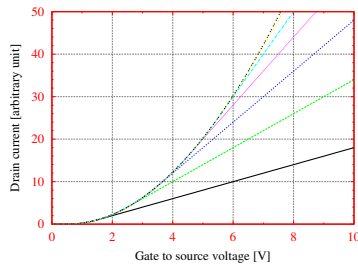
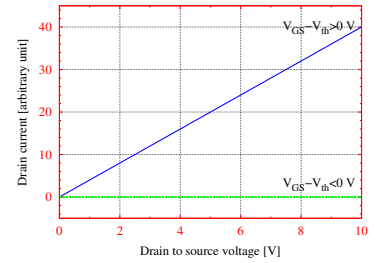
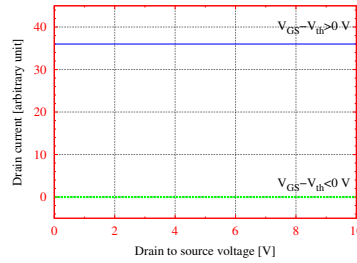
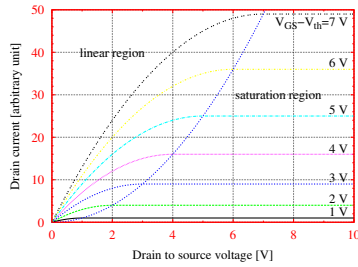
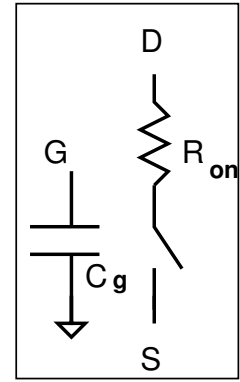
N-type MOSFET



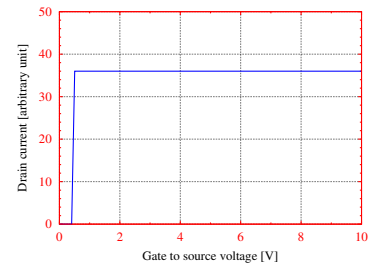
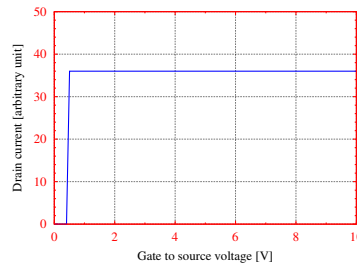
Zero-Order Model



First-Order Model



$I_{ds}$  unbounded when  $V_{gs} > V_{th}$



(even this is a simplified approximation)

Step at  $V_{gs} = V_{th}$

Reminder:

	NMOS	PMOS
Threshold	$V_{thn} > 0$	$V_{thp} < 0$ $V_{thp} \approx -V_{thn}$
Conduct	positive input $V_{gs} > V_{thn}$	negative input $V_{gs} < V_{thp}$
Drain	most positive terminal	most negative terminal
Source	most negative terminal (source of electrons)	most positive terminal (source of holes)

$$V_{gs} = V_g - V_s \tag{1}$$