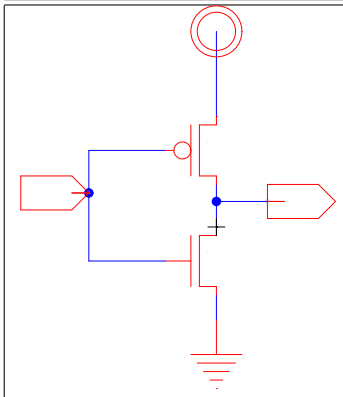
Let:

- R_0 – equivalent resistance of minimum size ($W = L = 1$) NMOS transistor
- I_0 – equivalent current of minimum size ($W = L = 1$) NMOS transistor
- C_0 – gate capacitance of minimum size transistor
- $\tau = R_0 C_0$ – technology-specific delay unit (maybe more accurate today $\tau = C_0/I_0$)

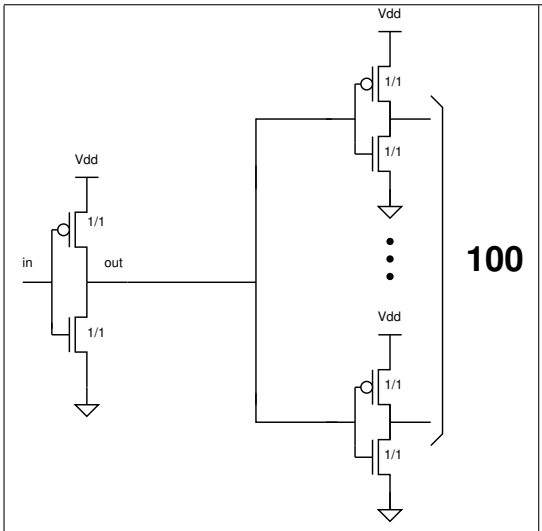
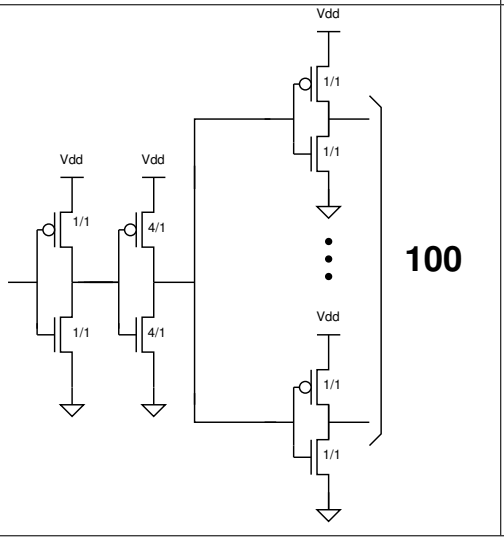
1. What are I_{ds}, R, and C in terms of I_0, R_0, and C_0 for a transistor with width W:

R_{drive}	
I_{drive}	
C_{gate}	

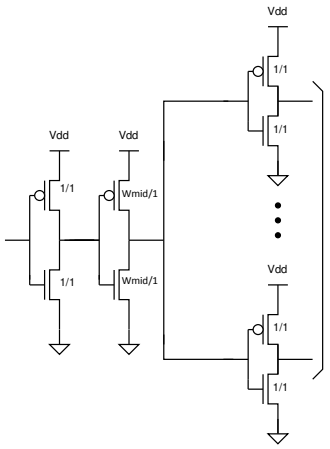
2. How size for equal rise/fall times assuming μ_n=500 cm$^2/(V \cdot s)$ and μ_p=200 cm$^2/(V \cdot s)$, velocity saturated, and $|V_{T_p}| = |V_{T_n}|$ and targeting $R_{drive} = \frac{R_0}{2}$.

	W_p	W_n	C_{in} in multiples of C_0
			

3. What is the delay in τ units?

	Delay
	
	

4. How should we size the transistors in middle stage to minimize delay?

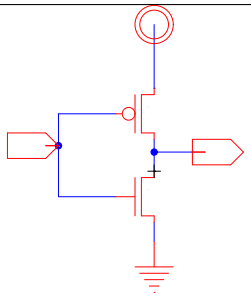
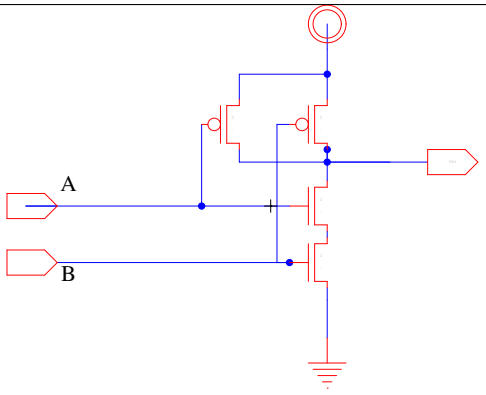
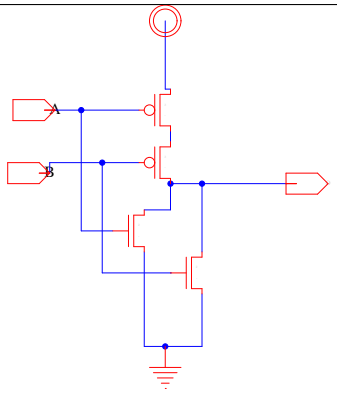
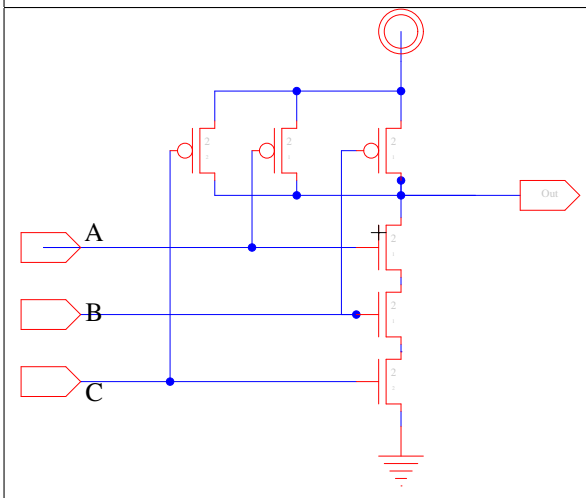
	W_p	W_n	Delay in τ
			

For following, assume:

(a) Extreme velocity saturation where $R_{p0} = R_{n0}$ (i.e. I_{ds} at rails is same for equally sized N and P devices—simplifying assumption we made for examples from last class)

(b) $R_{p0} = 2R_{n0}$ (i.e. I_{ds} PMOS at rails is half I_{ds} of NMOS)

5. How can you size for equal, worst-case rise/fall times assuming targeting $R_{drive} = \frac{R_0}{2}$ for the two cases above? C_a is the capacitance of the A input.

	$R_{p0} = R_{n0}$			$R_{p0} = 2R_{n0}$		
	W_p	W_n	C_a	W_p	W_n	C_a
	2	2	$4C_0$	4	2	$6C_0$
						
						
						

6. For a k-input NAND gate, sized for equal, worst-case rise/fall times and targeting $R_{drive} = \frac{R_0}{2}$:

	$R_{p0} = R_{n0}$	$R_{p0} = 2R_{n0}$
What is C_{in} as a function of k?		

7. Assuming sized for $\frac{R_0}{2}$ drive as above, and input also driven by $R_{drive} = \frac{R_0}{2}$, compare the delay of the following three nand32 implementations for the $R_{p0} = R_{n0}$ case. Include the delay of driving the input and assume each implementation has an output load of $4C_0$.

Organization	**Delay**
single-stage nand32