ESE 568: Mixed Signal Design and Modeling

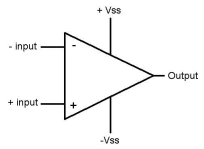
Lec 5: September 17th, 2018

Basic 2-stage Opamp Design

Opamp

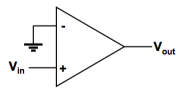
Ideal Opamp

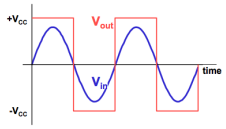
- The ideal opamp characterized by seven properties
  - Knowledge of these properties is sufficient to design and analyze a large number of useful circuits
- Basic opamp properties
  - Infinite open-loop voltage gain
  - Infinite input impedance
  - Zero output impedance
  - Zero noise contribution
  - Zero DC output offset
  - Infinite bandwidth
  - Differential inputs that stick together
    - Zero input differential voltage



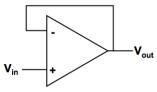
Opamp Practical Circuits

- Voltage comparator





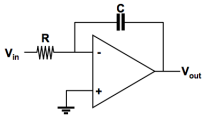
- Voltage follower



$V_{out} = V_{in}$

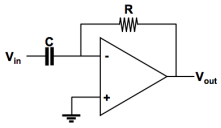
Opamp Practical Circuits

- Integrating amplifier



$$V_{out} = -\frac{1}{RC}\int V_{in}\,dt$$

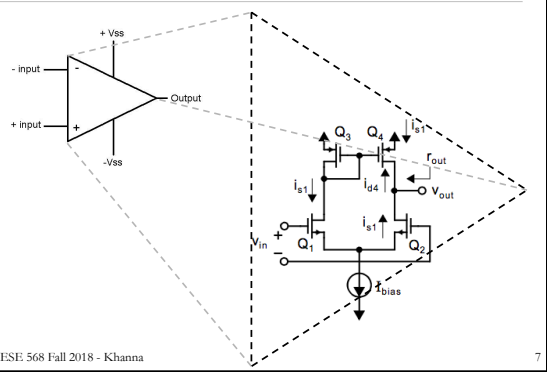
- Differentiating amplifier



$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Opamp Design

Ideal Opamp



Steps in Designing a CMOS Opamp

- 1) Choosing or creating the basic structure of the opamp
  - This step results in a schematic showing the transistors and their interconnections
  - This diagram does not change throughout the remainder of the design unless the specifications cannot be met, then a new or modified structure must be developed
- 2) Selection of the dc currents and transistor sizes
  - a.k.a Biasing and sizing
  - Most of the effort of design is in this category
  - Simulators are used to aid the designer in this phase

Steps in Designing a CMOS Opamp

- 3) Physical implementation of the design
  - Layout of the transistors
  - Floorplanning the connections, pin-outs, power supply buses and grounds
  - Extraction of the physical parasitics and re-simulation
  - Verification that the layout is a physical representation of the circuit
- 4) Fabrication
- 5) Measurement
  - Verification of the specifications
  - Modification of the design as necessary
    - Make sure it's not necessary!

Design Variables

- Boundary conditions (constraints):
  - 1. Process specification (V_T, μ, C_{ox}, etc.)
  - 2. Supply voltage and range
  - 3. Supply current and range
  - 4. Operating temperature and range

Design Variables

- Specifications:
  - 1. Open-loop Gain
  - 2. Gain bandwidth
  - 3. Settling time
  - 4. Slew rate
  - 5. Input common-mode range, ICMR
  - 6. Common-mode rejection ratio, CMRR
  - 7. Power-supply rejection ratio, PSRR
  - 8. Output-voltage swing
  - 9. Output resistance
  - 10. Offset
  - 11. Noise
  - 12. Layout area

Specifications

- 1. Open-loop Gain
  - Typically an op-amp may have a maximal open-loop gain of around 10^5

$$A_{OL} = \frac{V_{out}}{V_{in}^{+} - V_{in}^{-}}$$

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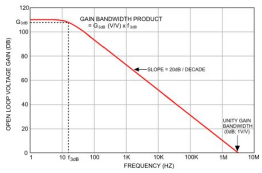
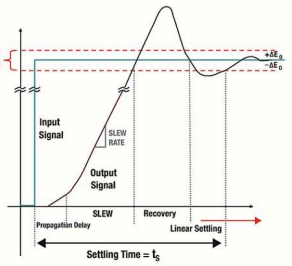
- 2. Gain bandwidth



Specifications

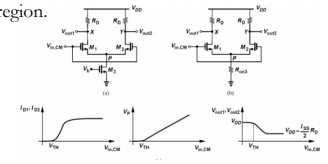
- 3. Settling time
- 4. Slew rate

$$SR = \max\left(\left|\frac{dv_{out}(t)}{dt}\right|\right)$$



Specifications

- 5. Input common-mode range, ICMR
  - The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.
  - Typically, the ICMR is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.



Specifications

- 6. Common-mode rejection ratio, CMRR
  - CMRR is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

$$CMRR = \frac{a_{vd}}{a_{vc}}$$

- 7. Power-supply rejection ratio, PSRR

$$PSRR_{+} = \frac{a_{vd}}{a_{+}}$$

$$PSRR_{-} = \frac{a_{vd}}{a_{-}}$$

Specifications

- 8. Output-voltage swing
  - Expected output swing
- 9. Output resistance
  - Resistance seen into the output
- 10. Offset
  - Output offset voltage (V_{OS}(out))
    - The output offset voltage is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

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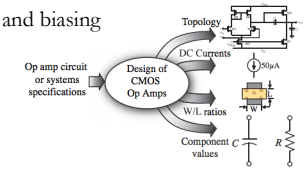
  - Input referred offset voltage (V_{OS}(in) = V_{OS})
    - The input referred offset voltage is equal to the output offset voltage divided by the differential voltage gain.
    - $V_{OS} = V_{OS}(out)/A_{VD}$

Opamp Design Output

- 1) The topology
- 2) The dc currents
- 3) The W and L values of transistors
- 4) The values of components

- I.e Schematic and biasing



Opamp Design Practical Advice

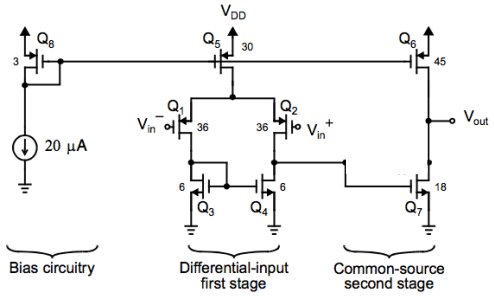
- 1) Decide upon a suitable topology
  - The topology should be the one capable of meeting most of the specifications
  - Try to avoid "inventing" a new topology but start with an existing topology
- 2) Determine the type of compensation needed to meet the specifications
  - Consider the load and stability requirements
  - Use some form of Miller compensation or a self-compensated approach
- 3) Design dc currents and device sizes for proper dc, ac, and transient performance
  - This begins with hand calculations based upon approximate design equations.
  - Compensation components are also sized in this step of the procedure.
  - After each device is sized by hand, a circuit simulator is used to fine tune the design

Opamp Design Practical Advice

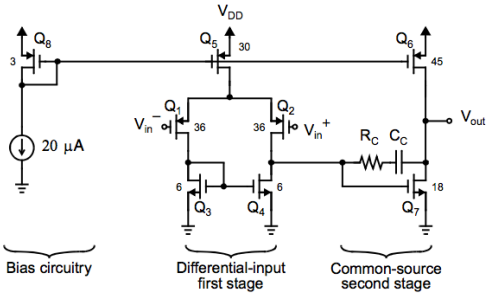
- Two basic steps of design:
  - 1) "First-cut" - this step is to use hand calculations to propose a design that has potential of satisfying the specifications. Design robustness is developed in this step.
  - 2) Optimization - this step uses the computer to refine and optimize the design.

Basic 2-stage Opamp

2-Stage Opamp



2-Stage Opamp



Design Variables

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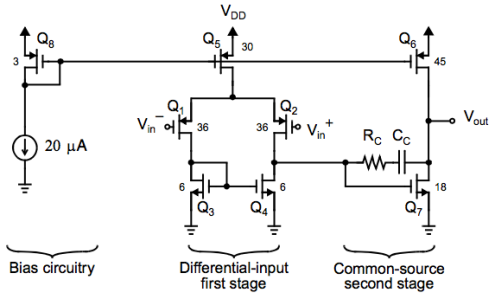
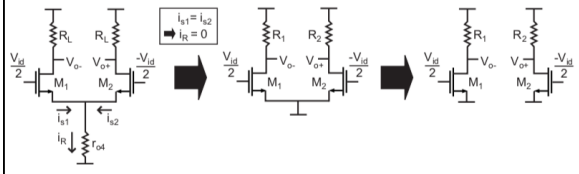
Basic 2-stage Opamp

2-Stage Opamp



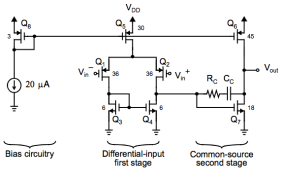
Differential DC Gain



- Inputs are equal in magnitude but opposite in sign to each other
- By linearity and symmetry, i_{s1} must equal $-i_{s2}$
  - This implies i_R is zero, so that voltage drop across ro4 is zero
    - The sources of M_1 and M_2 are therefore at incremental ground and decoupled from each other!

2-Stage Opamp

- 1. Open-loop Gain

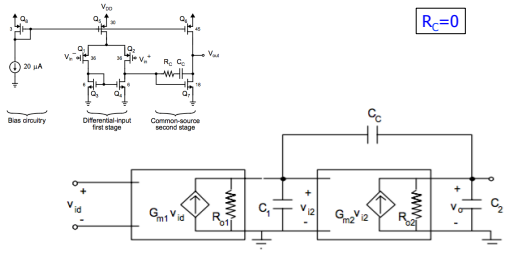


$$A_{v1} = -g_{m1}(r_{ds2} \| r_{ds4})$$

$$A_{v2} = -g_{m7}(r_{ds6} \| r_{ds7})$$

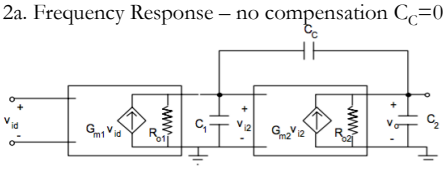
2-Stage Opamp

- 2. Frequency Response



2-Stage Opamp

- 2a. Frequency Response – no compensation C_C=0



- Two poles:

$$p_1 = -\frac{1}{R_{o1}C_1} \qquad p_2 = -\frac{1}{R_{o2}C_2}$$

2-Stage Opamp

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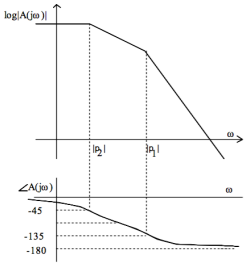
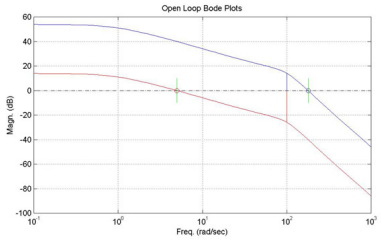


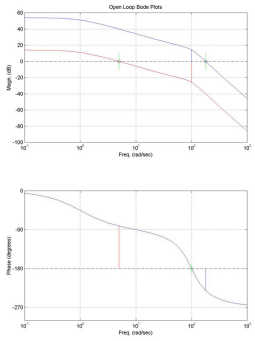
$$p_1 = -\frac{1}{R_{o1}C_1} \qquad p_2 = -\frac{1}{R_{o2}C_2}$$

$$A(s) = \frac{A_0}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}$$

2-Stage Opamp Transfer Functions

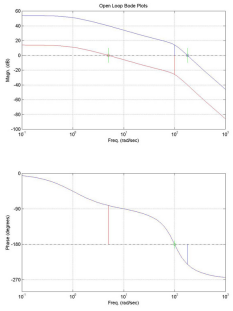


2-Stage Opamp Transfer Functions



Phase Margin

- Find phase at unity-gain frequency (ω_0)
- Add 180° for phase margin
- Red
  - Phase at ω_0 = −81.3°
  - PM=98.7°
- Blue
  - Phase at ω_0 = −231°
  - PM=-50°



Stability

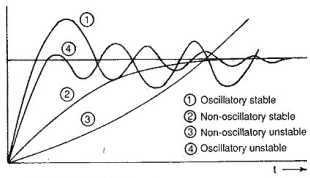
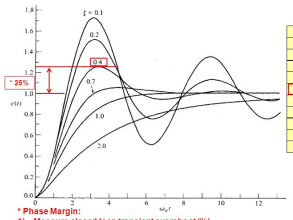


Fig. 6.11(a) *Typical transient responses of systems*

Stability vs. Phase Margin

2nd Order Transient Curves



Overshoot (%)	Phase Margin (deg)
10	57.5
15	50
20	42.5
* 25	40
30	35
35	32.5
40	30
45	27.5
50	25

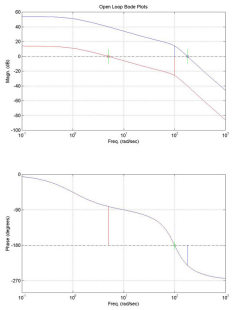
* Phase Margin:
1) Measure closed loop transient overshoot (%)
2) Find overshoot on graph above and read closest damping ratio, ζ
3) Use damping ratio, ζ, or Overshoot (%) to find phase margin using Slide 75 graph

From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

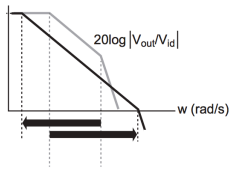
Texas Instruments

Phase Margin

- Find phase at unity-gain frequency (ω_0)
- Add 180° for phase margin
- Want phase margin >45° (~60°)
  - Problem: Hard to do with 2-stage opamp with high gain
  - Solution: Split the poles



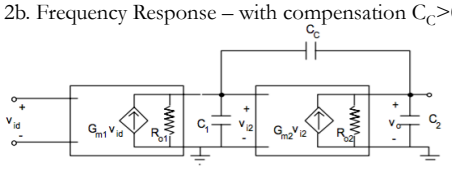
Impact of Pole Splitting with Compensation Cap



- Pole splitting allows the dominant pole frequency to be dramatically decreased and the main parasitic pole to be dramatically increased
  - We can achieve higher unity gain frequency with improved phase margin

2-Stage Opamp

- 2b. Frequency Response – with compensation C_C>0

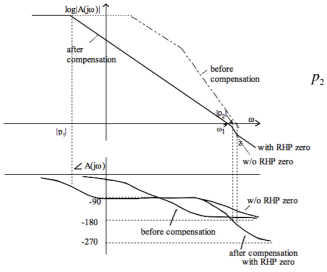


  - Two poles:

$$p_1 \approx -\frac{1}{R_{o1}(g_{m7}R_{o2}C_C)} \qquad p_2 \approx -\frac{g_{m7}C_C}{C_1C_2+C_1C_C+C_CC_2} \approx \frac{-g_{m7}}{C_2}$$

2-Stage Opamp

- 2b. Frequency Response – with compensation C_C>0



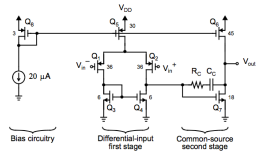
$$p_1 \approx -\frac{1}{R_{o1}(g_{m7}R_{o2}C_C)}$$

$$p_2 \approx -\frac{g_{m7}C_C}{C_1C_2+C_1C_C+C_CC_2} \approx \frac{-g_{m7}}{C_2}$$

$$z_1 = \frac{g_{m7}}{C_C}$$

$$A(s) = \frac{A_0\left(1-\frac{s}{z_2}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}$$

Nulling Resistor

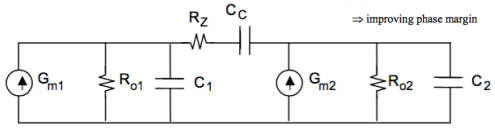


$$z_1 = \frac{1}{C_C\left(\left|\frac{1}{G_{m2}}\right| - R_Z\right)}$$

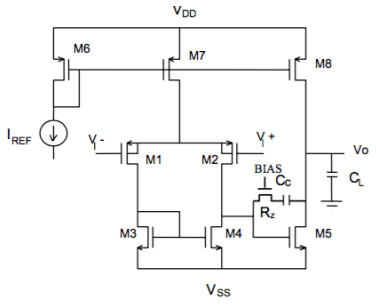
If $R_Z = \left|\frac{1}{G_{m2}}\right|$, zero cancelled

If $R_Z > \left|\frac{1}{G_{m2}}\right|$, zero moves to left half-plane

⇒ improving phase margin

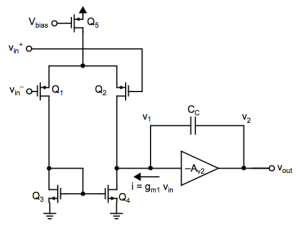


Transistor for R_Z



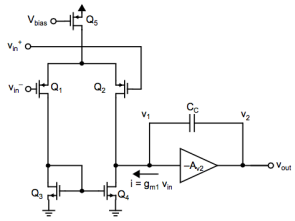
2-Stage Opamp – Unity Gain Freq

- Equivalent capacitance at node v_1



2-Stage Opamp – Unity Gain Freq

- Equivalent capacitance at node v_1: $C_{eq} = C_C(1+A_{v2}) \approx C_C A_{v2}$



2-Stage Opamp – Unity Gain Freq

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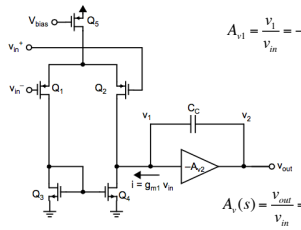


$$A_{v1} = \frac{v_1}{v_{in}} = -g_{m1} Z_{out1} = -g_{m1}\left(r_{ds2} \,\|\, r_{ds4} \,\|\, \frac{1}{sC_{eq}}\right)$$

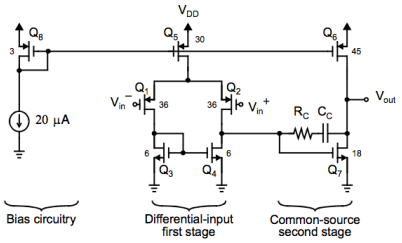
$$A_{v1} \cong -g_{m1}\frac{1}{sC_{eq}} \cong -g_{m1}\frac{1}{sC_C A_{v2}}$$

$$A_v(s) = \frac{v_{out}}{v_{in}} = A_{v2}A_{v1} \cong A_{v2}\frac{-g_{m1}}{sC_C A_{v2}} = \frac{-g_{m1}}{sC_C}$$

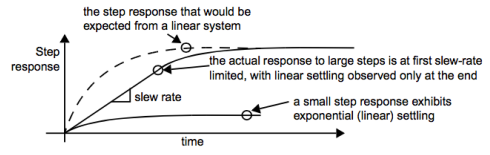
$$\left|A_v(j\omega_0)\right| = 1 \quad \text{for} \quad \omega_0 = \frac{g_{m1}}{C_C}$$

2-Stage Opamp

- 3/4. Settling Time/Slew Rate

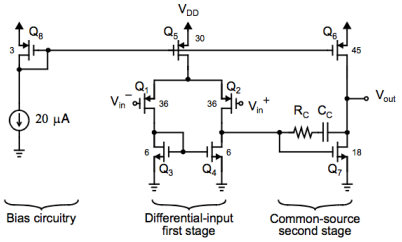


2-Stage Opamp – Slew Rate



2-Stage Opamp

- 3/4. Settling Time/Slew Rate



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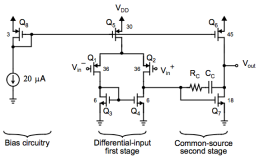
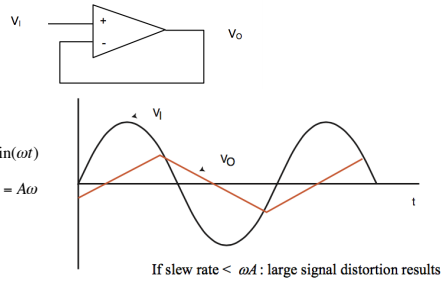


$$SR \equiv \left.\frac{dv_{out}}{dt}\right|_{\max} = \frac{I_{C_C}|_{\max}}{C_C} = \frac{I_{D5}}{C_C}$$

Finite Slew Rate Effect

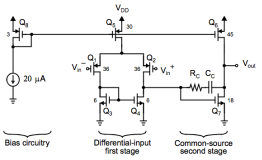
- Ex. Unity-gain Follower



If slew rate < ωA : large signal distortion results

2-Stage Opamp

- 3/4. Settling Time/Slew Rate



$$SR \equiv \left.\frac{dv_{out}}{dt}\right|_{\max} = \frac{I_{C_C}|_{\max}}{C_C} = \frac{I_{D5}}{C_C}$$

$$\omega_0 = \frac{g_{m1}}{C_C}$$

Unity Gain Freq and Slew Rate

- Relationship between unity gain frequency and slew rate:

$$\omega_0 = \frac{g_{m1}}{C_C} \qquad SR = \frac{I_{D5}}{C_C} \quad \Rightarrow \quad SR = \frac{I_{D5}}{g_{m1}}\omega_0$$

- For 45° phase margin: $\omega_o = |p_2|$

$$SR = \frac{I_{D5}}{g_{m1}}|p_2|$$

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$$p_2 \approx -\frac{g_{m7}C_C}{C_1C_2 + C_1C_C + C_CC_2} \approx \frac{-g_{m7}}{C_2}$$

Design Variables

- Specifications:
  - 1. Open-loop Gain
  - 2. Gain bandwidth
  - 3. Settling time
  - 4. Slew rate
  - 5. Input common-mode range, ICMR
  - 6. Common-mode rejection ratio, CMRR
  - 7. Power-supply rejection ratio, PSRR
  - 8. Output-voltage swing
  - 9. Output resistance
  - 10. Offset
  - 11. Noise
  - 12. Layout area

Admin

- HW 2 and 3 due Su
  - Want to make sure every has Cadence set up and running