University of Pennsylvania
Department of Electrical and System Engineering
Digital Integrated Cicruits AND VLSI Fundamentals

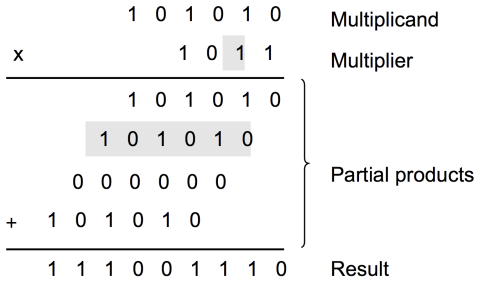
ESE570, Fall 2021 HW 7: 4x4 Array Multiplier Monday, October 18

Homework Due: Monday, October 25, 11:59PM

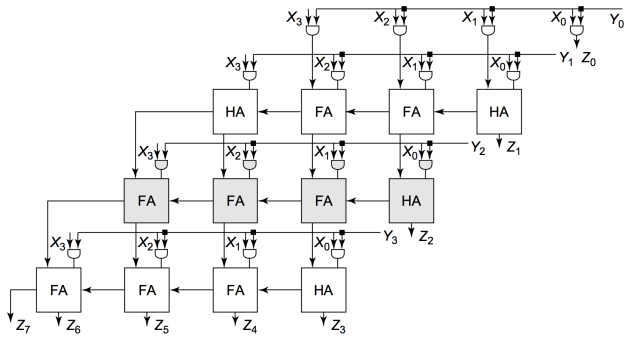
Design Problem: Design the circuit-level implementation of a full-adder bit-slice (for a 4x4 array multiplier).

- Your design will be completed in our .6u technology in Cadence
- Your design must be cascadable to build adders useable in multipliers.
- You must stay with a cascadable, bit-slice, design for this assignment.
- You may also design a half-adder (no C_{in} input) for use in the multiplier array for delay reduction. Nonetheless, the number of cell types needed should be a small constant number.

Binary Multiplication: Binary multiplication is done by doing additions. Partial products are calculated by multiplying the multiplicand by each bit of the multiplier and then summing the partial products. An example is shown below:



To implement the multiplication, you will design an array multiplier that multiplies two 4-bit inputs and calculates an 8-bit output. The array is shown below where X and Y are the inputs and Z is the output:



Baseline Design: You will create a design for your multiplier with all minimum sized devices and then modify your baseline into a delay-optimized design, which is discussed below.

- CMOS design: Use CMOS logic discipline, 5V= V_{dd}, and minimum size transistors.
- The design you implement must be measured with the following 2 design metrics:
  - *delay*: Measure the delay of a 4bx4b multiplication. This is the worst-case delay from two 4b inputs to all 8b of output. Load the outputs by the equivalent load as the input to your multiplier. Drive the inputs by the equivalent drive of one of your multipliers. You must consider what input case would give the worst case delay.
  - *maximum active energy*: Measure the energy for the 4x4 multiplication when all inputs switch from $0 \rightarrow 1$)
- With your homework, you should submit:
  - All schematics for your design, including test schematics
  - Description of operation of your design
  - Verified logical correctness of both your bit-slice(s) and array multiplier
  - Description of the input case for worst-case delay and why it gives the worst case delay.
  - Summary of the design metrics for design. Include supporting evidence in the form of equations and simulation results.

  Hint: Verify design in components. Test bit-slice before full multiplier.

Optimized Design: You will modify your Baseline Design into a delay-optimized design.

- You select gate structure, gate types, transistor sizes, and logic discipline (CMOS, ratioed, or pass logic).
- You may use any $V_{dd} \leq 5.0$V.
- With your homework, you should submit:
  - All schematics for your optimized design, including test schematics
  - Verified logical correctness of both your bit-slice and array multiplier in the optimized design
  - Summary of the 2 design metrics (delay and active energy)
  - A brief description of how you optimized your design
  - Describe and discuss a comparison of your baseline and optimized design metrics

There is a reference for multipliers in Canvas files for more detailed information.