# ESE 570: Digital Integrated Circuits and VLSI Fundamentals

Lec 14: March 1, 2016

Combination Logic: Ratioed and Pass Logic



## Lecture Outline

- CMOS Gates Review
  - CMOS Worst Case Analysis
- Ratioed Logic Gates
- Pass Transistor Gates



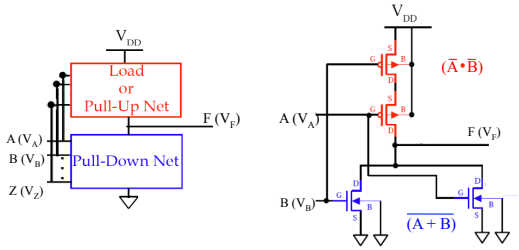
## Review: 1st Order RC Delay Models

$$\tau_{PHL} \approx 0.69 \cdot C_{load} \cdot R_n \qquad C_{load} \approx C_{dbn} + C_{dbp} + C_{int} + C_{gb}$$

- Equivalent circuits used for MOS transistors
  - Ideal switch + "effective" ON resistance + load capacitance
    - Define unit resistance, $R_u$: "effective" ON resistance of transistor with min length and W=$W_n$ (usually min width)
    - nMOS has "effective" ON resistance $R_n = R_{un}/\kappa_n$ and capacitances $\kappa_n C_d$, $\kappa_n C_g$
    - pMOS has "effective" ON resistance $R_p = R_{up}/\kappa_p$ and capacitances $\kappa_p C_d$, $\kappa_p C_g$
      - scale factors $\kappa_n \geq 1$ and $\kappa_p \geq 1$, i.e. $W_n = \kappa_n W_{un}$, $W_p = \kappa_p W_{up}$
    - $C_{gb} = C_g$ and $C_{db} = C_{sb} = C_d$ for the unit n/pMOS transistors
  - NMOS and pMOS transistor at minimum gate length (L)
    - Capacitance directly proportional to gate width (W) → C = W*C
    - Conductance directly proportional to gate width (W) → G = W*G
    - Resistance is inversely proportional to gate width (W) → R = R/W



## Review: Two-Input NOR Gate (NOR2)




For Complimentary CMOS: Pull-up Net = dual (Pull-down Net)

$(\bar{A} \cdot \bar{B}) = \overline{(A + B)}$



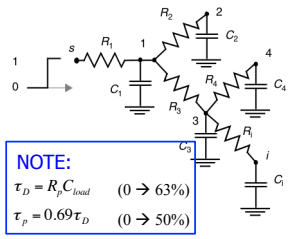
## Review: Elmore Delay: Distributed RC network

- The delay from source to node *i*
  - N = number of nodes in circuit

$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow 4) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

$$\tau_{Di} = C_1(R_1) + C_2(R_1) + C_3(R_1 + R_3) + C_4(R_1 + R_3) + C_i(R_1 + R_3 + R_i)$$



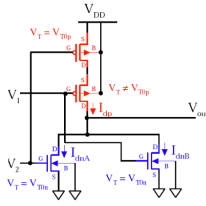

NOTE:

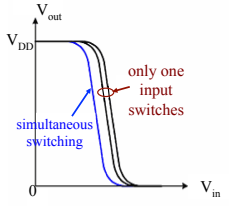
$\tau_D = R_p C_{load}$ (0 → 63%)

$\tau_p = 0.69 \tau_D$ (0 → 50%)



## CMOS NOR2 VTC




3 VTC Cases

$V_1 = 0$ V; $V_2 = 0 \rightarrow V_{DD}$

$V_1 = 0 \rightarrow V_{DD}$; $V_2 = 0$

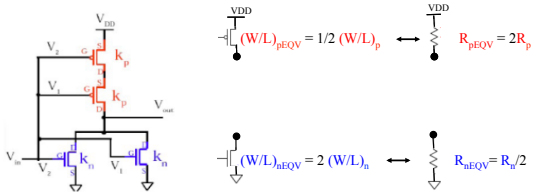
$V_1$ and $V_2 = 0 \rightarrow V_{DD}$ simultaneously

Switching Threshold Voltage:

$V_1 = V_2 = V_{out} = V_{th}$

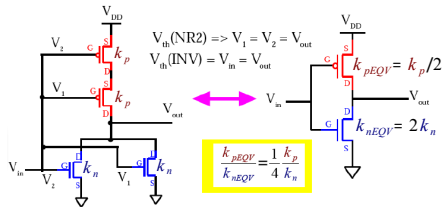
## Switch-RC Transistor Models

2-input NOR Nets






## CMOS NOR2 $V_{th}$






## Review: CMOS Inverter: $V_{th}$

$$\frac{k'_n}{2}\left(\frac{W}{L}\right)_n (V_{in}-V_{TOn})^2 = \frac{k'_p}{2}\left(\frac{W}{L}\right)_p (V_{in}-V_{DD}-V_{TOp})^2$$

$$k_R (V_{th}-V_{TOn})^2 = (V_{th}-V_{DD}-V_{TOp})^2$$

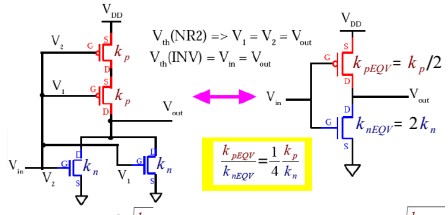
$$V_{th} = \frac{V_{TOn} + \sqrt{\frac{1}{k_R}}(V_{DD}+V_{TOp})}{1+\sqrt{\frac{1}{k_R}}}$$

Typically, $L_n = L_p = L_{min}$

$$k_R = \frac{k'_n (W/L)_n}{k'_p (W/L)_p} = \frac{\mu_n (W/L)_n}{\mu_p (W/L)_p} = \frac{\mu_n W_n}{\mu_p W_p}$$



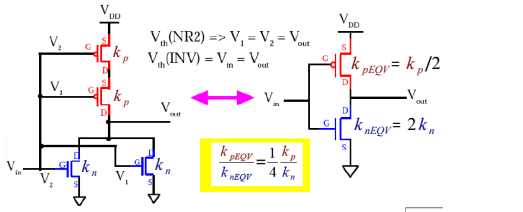
## CMOS NOR2 $V_{th}$




$$V_{th}(NR2) = \frac{V_{TOn} + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}(V_{DD}+V_{Top})}{1+\frac{1}{2}\sqrt{\frac{k_p}{k_n}}} \quad \leftrightarrow \quad V_{th}(EQINV) = \frac{V_{TOn} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}(V_{DD}+V_{Top})}{1+\sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$



## CMOS NOR2 $V_{th}$




Symmetric 'Inv'

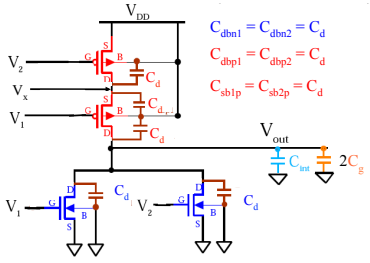
$$V_{th} = \frac{V_{DD}}{2} \quad \& \quad \frac{k_{pEQV}}{k_{nEQV}} = 1$$

$$k_p = 4k_n$$

$$V_{th}(EQINV) = \frac{V_{TOn} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}(V_{DD}+V_{Top})}{1+\sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$



## Parasitic Caps for NOR2 (worst case)



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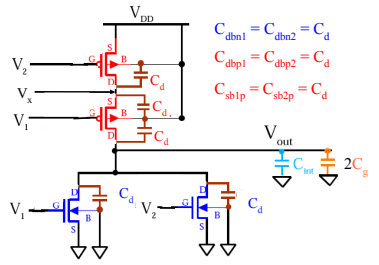
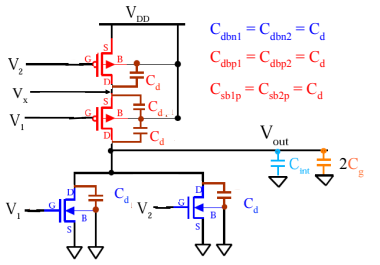



WORST CASE for PULL-UP => $V_1 = 0, V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> $V_{DD}$



## Parasitic Caps for NOR2 (worst case)




WORST CASE for PULL-UP => $V_1 = 0, V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> $V_{DD}$

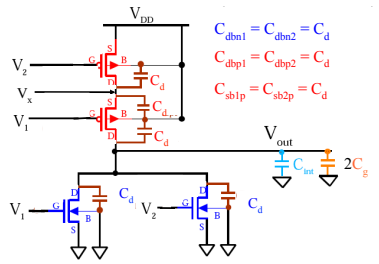
$C_{load\text{-}NR2} \approx 2C_d + 3C_d + C_{int} + 2C_g$

$R_{pEQV} = R_{p2}+R_{p1}$

Lumped Model



## Parasitic Caps for NOR2 (worst case)




WORST CASE for PULL-UP => $V_1 = 0, V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> $V_{DD}$

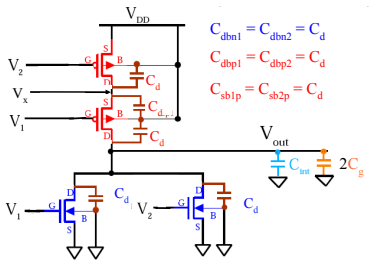
$C_{load\text{-}NR2} \approx 2C_d + 3C_d + C_{int} + 2C_g$

$R_{pEQV} = R_{p2}+R_{p1}$

Elmore Model?



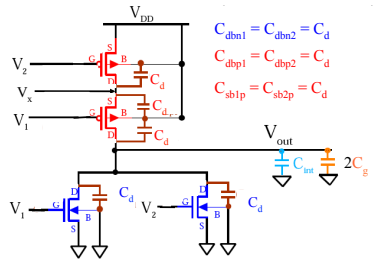
## Parasitic Caps for NOR2 (worst case)




WORST CASE for PULL-DOWN => $V_1 = 0, V_2 = 0$ ->$V_{DD}$ @t=0 & $V_x \approx V_{out}$=$V_{DD}$-> 0



## Parasitic Caps for NOR2 (worst case)



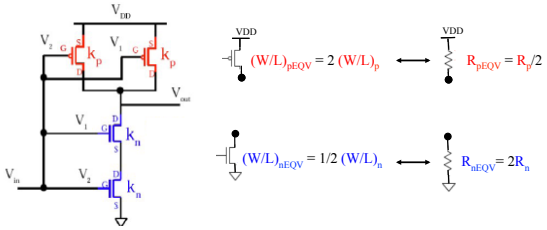

WORST CASE for PULL-DOWN => $V_1 = 0, V_2 = 0$ ->$V_{DD}$ @t=0 & $V_x \approx V_{out}$=$V_{DD}$-> 0

Elmore Model?

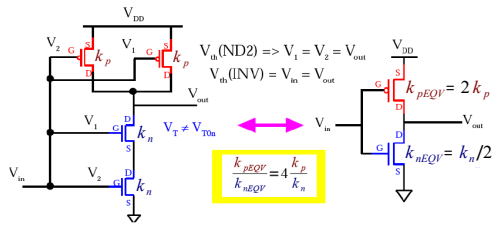


## Switch-RC Transistor Models

2-input NAND Nets



## CMOS NAND2 $V_{th}$






## CMOS NAND2 $V_{th}$




$$V_{th}(ND2) = \frac{V_{T0n} + 2\sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{T0p})}{1 + 2\sqrt{\frac{k_p}{k_n}}} \quad V_{th}(EQINV) = \frac{V_{T0n} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}(V_{DD} + V_{T0p})}{1 + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$



## CMOS NAND2 $V_{th}$




Symmetric 'Inv'

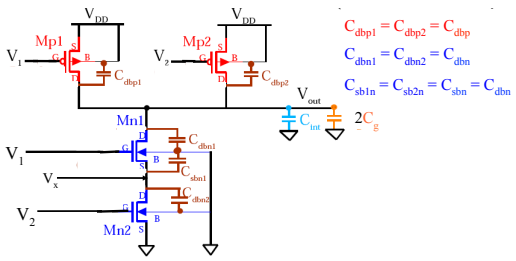
$$V_{in} = \frac{V_{DD}}{2} \quad \& \quad \frac{k_{pEQV}}{k_{nEQV}} = 1$$

$$4k_p = k_n$$

$$V_{th}(EQINV) = \frac{V_{T0n} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}(V_{DD} + V_{T0p})}{1 + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}}$$



## Parasitic Caps for NAND2 (worst case)



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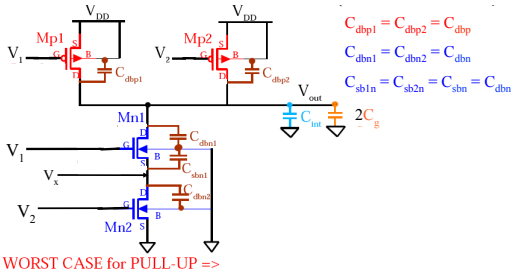
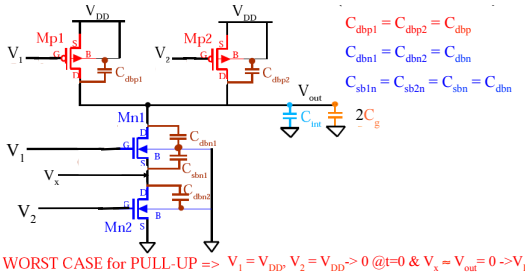



WORST CASE for PULL-UP =>

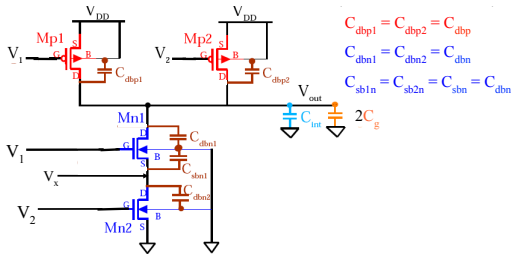


## Parasitic Caps for NAND2 (worst case)




WORST CASE for PULL-UP => $V_1 = V_{DD}$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ ->$V_{DD}$

## Parasitic Caps for NAND2 (worst case)




$C_{dbp1} = C_{dbp2} = C_{dbp}$

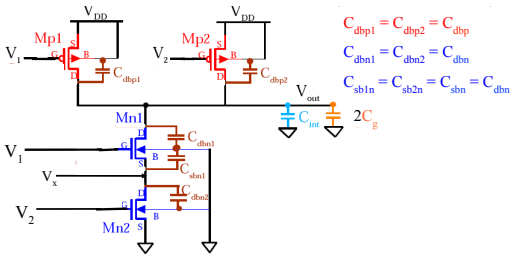
$C_{dbn1} = C_{dbn2} = C_{dbn}$

$C_{sb1n} = C_{sb2n} = C_{sbn} = C_{dbn}$

WORST CASE for PULL-DOWN =>



## Parasitic Caps for NAND2 (worst case)




$C_{dbp1} = C_{dbp2} = C_{dbp}$

$C_{dbn1} = C_{dbn2} = C_{dbn}$

$C_{sb1n} = C_{sb2n} = C_{sbn} = C_{dbn}$

WORST CASE for PULL-DOWN => $V_1 = V_{DD}$, $V_2 = 0 \rightarrow V_{DD}$ @t=0 & $V_x \approx V_{out} = V_{DD} \rightarrow 0$



## Ratioed Logic



## Previously

- Restoration and Noise Margins
  - Allows for gate abstraction
- CMOS Gates
  - Drive outputs rail-to-rail
  - Only one network turned on in steady state
    - Only subthreshold leakage current in steady state



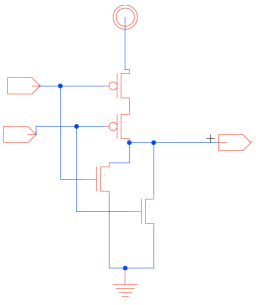
## Today

- Ratioed Gates
  - Break all the rules… (nice properties)
    - No rail-to-rail outputs, steady-state-current is not subthreshold…
  - Logic correctness
  - Performance
  - Power
  - Implications



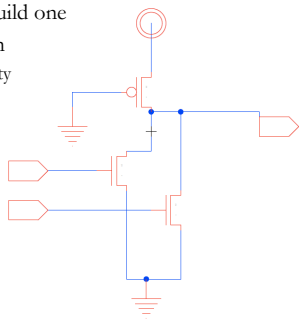
## Idea

- Building both pull-up and pull-down can be expensive – many gates
- Seems wasteful to build logic function twice
  - Once in pullup, once in pulldown
  - Large gate capacitance



## Idea

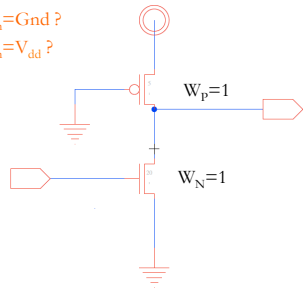
- Maybe only need to build one
- Build NFET pulldown
  - Exploit high N mobility
    - traditional





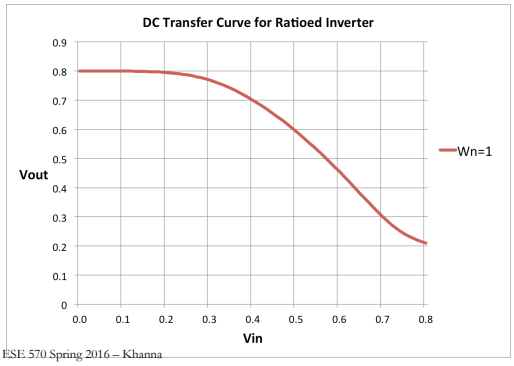
## Ratioed Inverter

- Does this work?
  - What is $V_{out}$ for $V_{in}$=Gnd ?
  - What is $V_{out}$ for $V_{in}$=$V_{dd}$ ?



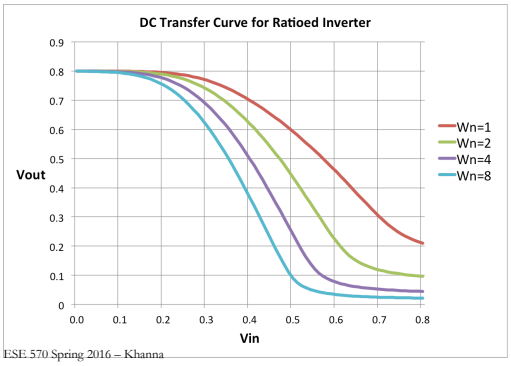



## Ratioed Inverter in 22nm



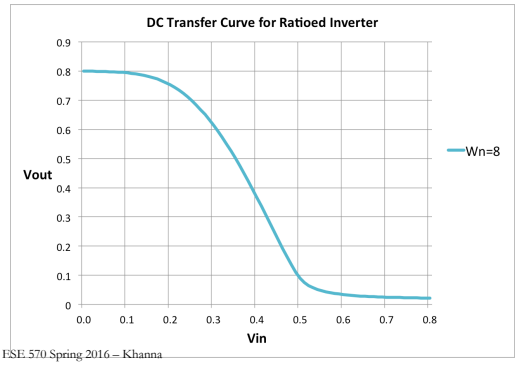



## Ratioed Inverter in 22nm





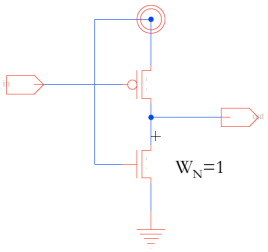

## DC Transfer Function



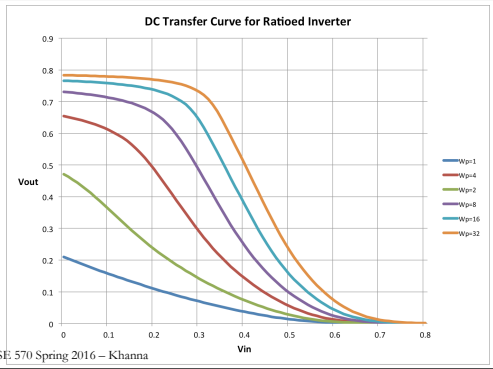



## Ratioed Inverter

- How do we need to size P to make it work?



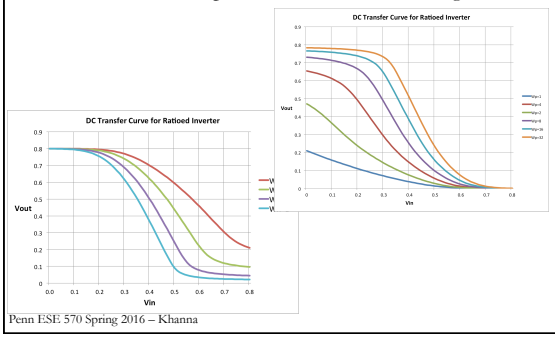
## Ratioed Inverter in 22nm






## P vs. N

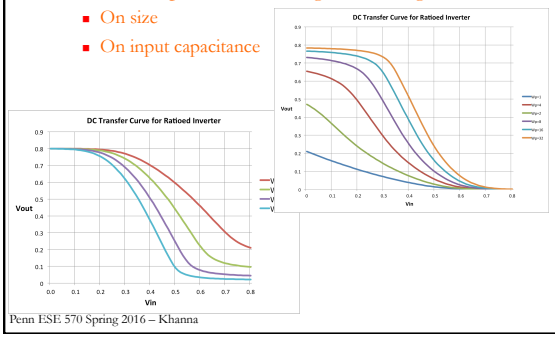
- **Conclude:** still prefer N to P for ratioed logic






## Noise Margin Tradeoff

- What is impact of increasing noise margin?
  - On size
  - On input capacitance



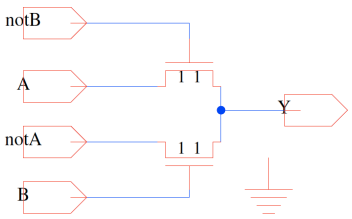



## Pass Transistor Logic




## Teaser

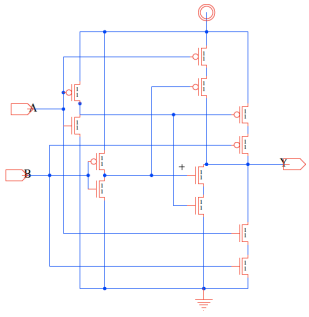
- What does this do?





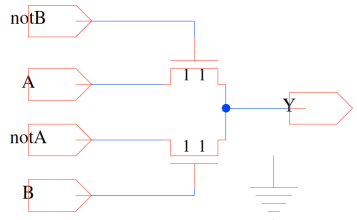

## Identify Function

- What function is this?



## Output

- What is Vout if A=1, B=1?

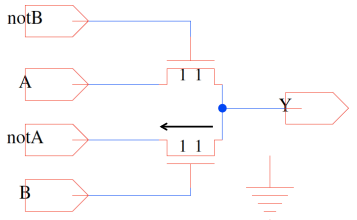



| A | B | Y |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |



## Output

- What is Vout if A=1, B=1?

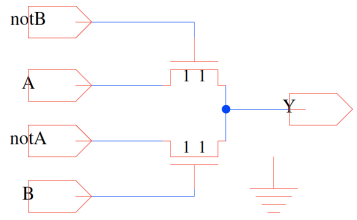



| A | B | Y |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | 0 |



## Output

- What is Vout if A=0, B=1?

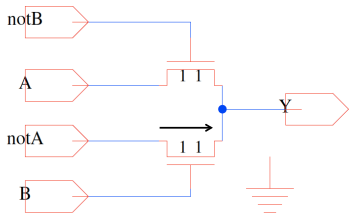



| A | B | Y |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | 0 |



## Output

- What is Vout if A=0, B=1?

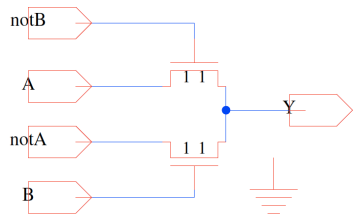



| A | B | Y |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | 1 |
| 1 | 0 | |
| 1 | 1 | 0 |



## Output

- What is Vout if A=0, B=0? if A=1, B=0?

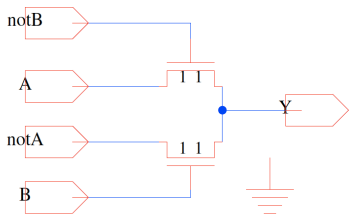



| A | B | Y |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | 1 |
| 1 | 0 | |
| 1 | 1 | 0 |



## Output

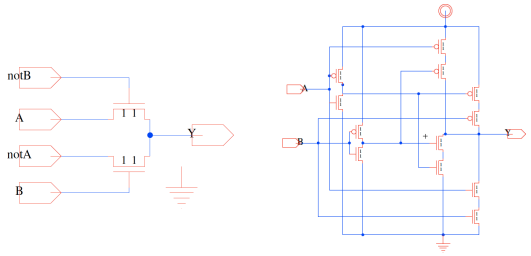
- What is Vout if A=0, B=0? if A=1, B=0?




| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## Area

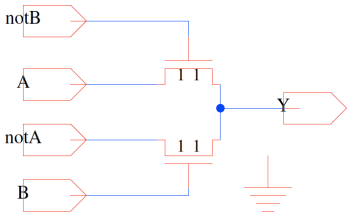
- Compare PT with CMOS circuit?






## Output

- Is this a regenerating/restoring gate?

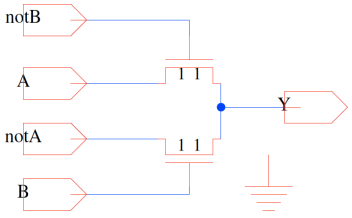



| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



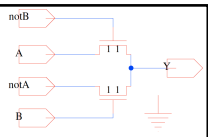
## Output

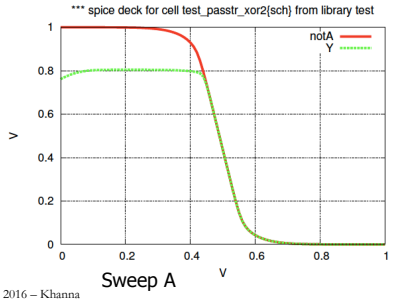
- What does output look like (DC transfer)?
  - (B=1, notB=0, sweep A, notA=CMOS inv(A))





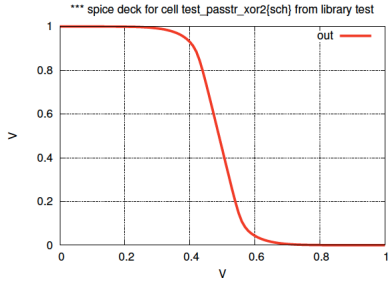

## Pass TR transfer (B=1)



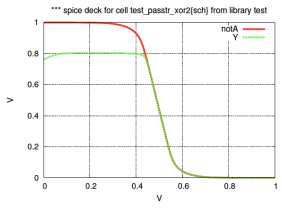


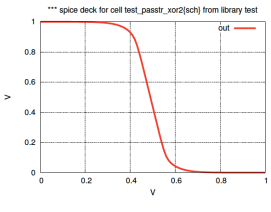

## CMOS Inverter Transfer



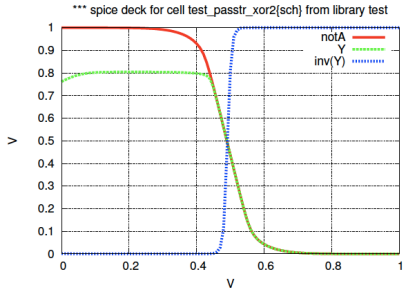



## Reasonable Input to CMOS Inverter?



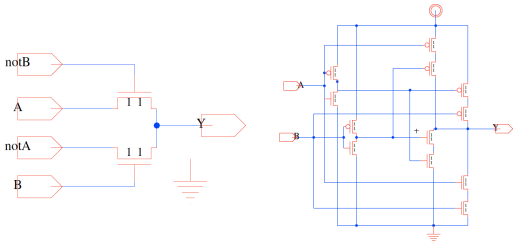
## Pass Transistor xor2 with inv restore






## Compare CMOS

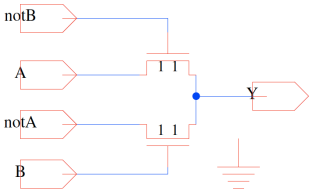
- Is this a fair comparison?





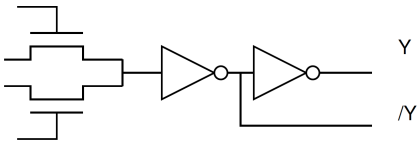

## Required to use?

- What should we add to make substitutable with CMOS?





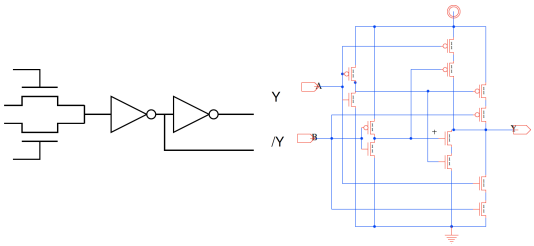

## Restore Output





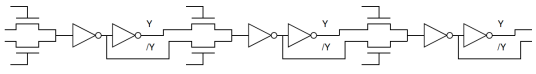

## Restore Output

- Area? (compare to CMOS)

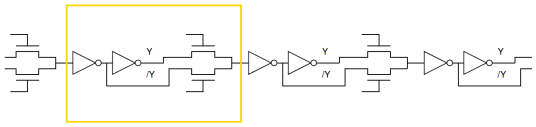





## Chain Together

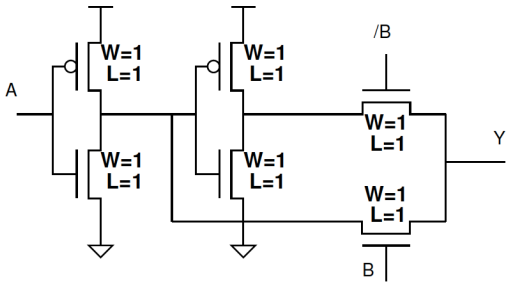


## Analyze Stage





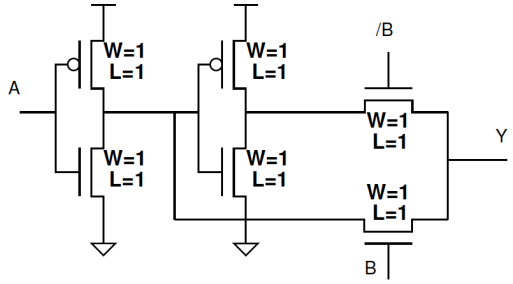

## Delay A=1, B=0, $C_{DB}$=$C_{diff}$=0?






## Delay A=1, B=0, $C_{diff}$=0?

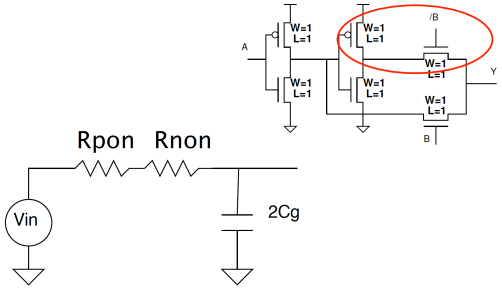
- What's the equivalent RC circuit?





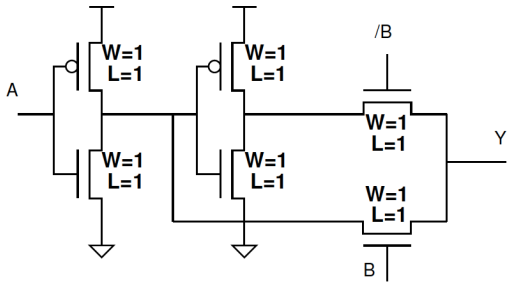

## Delay A=1, B=0, $C_{diff}$=0?

- What's the equivalent RC circuit?





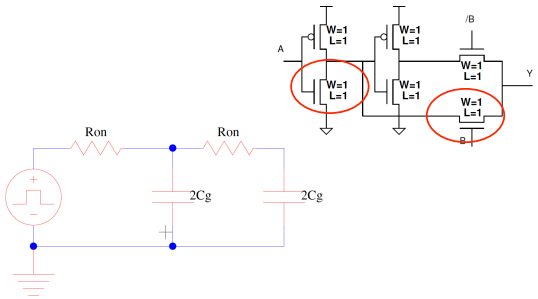

## Delay A=1, B=1, $C_{diff}$=0?





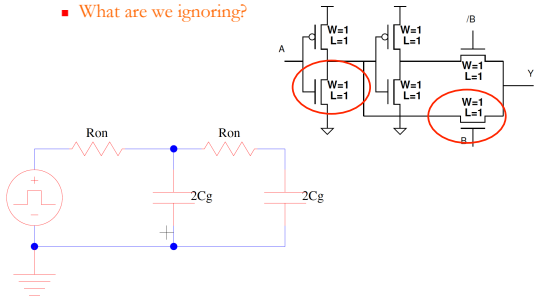

## Delay A=1, B=1, $C_{diff}$=0?

- What's the equivalent RC circuit?



## Delay A=1, B=1, $C_{diff}$=0?

- What's the equivalent RC circuit?
  - What are we ignoring?





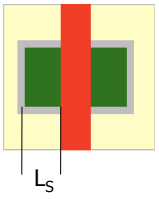

## $C_{diff}$>0



## Contact/Diffusion Capacitance

- $C_j$ – diffusion depletion
- $C_{jsw}$ – sidewall capacitance
- $L_S$ – length of diffusion

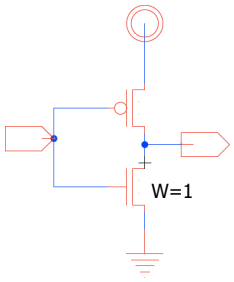
$$C_{diff} = C_j L_S W + C_{jsw}(2L_S + W)$$





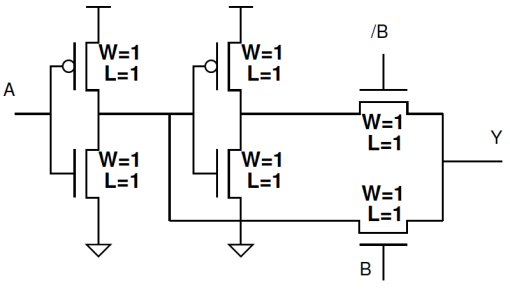

## Inverter Delay

- Delay driving another min-sized inverter?
  - Include $C_{diff}$





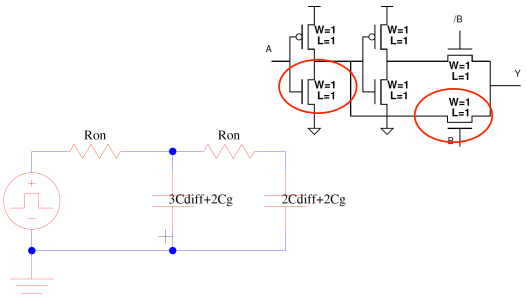

## Delay A=1, B=1, $C_{diff}$≠0? (W=1)





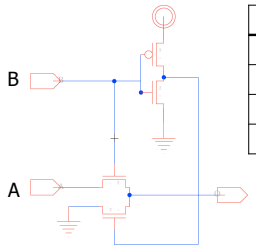

## Delay A=1, B=1, $C_{diff}$≠0? (W=1)

- What's the equivalent RC circuit?



## Bonus

- What does this do?




| A | B | Y |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |



## Idea

- CMOS Logic
  - Complimentary dual pull-up/down networks
- There are other logic disciplines
  - We have the tools to analyze
- Ratioed Logic
  - Tradeoff noise margin for
    - Reduced area? Capacitive load?
  - Dissipates static power in one mode
- Can use pass transistors for logic
  - Sometimes gives area or delay win



## Midterm Exam

- Midterm – 3/15
  - In class
    - Starts at exactly 4:30pm, ends at exactly 5:50pm (80 minutes)
  - Location TBD, posted on Piazza and Course Calendar
  - Covers Lec 1- 14 (slides 1-26)
  - Closed book, no notes or cheat sheets
  - Calculators allowed
  - Review Session by TA on Sunday 3/13 - time and location TBD
  - Extra office hours on Monday (3/14) and Tuesday (3/15) (time and location TBD)



## Admin

- HW 5 due Thursday, 3/3
- Di and Ao OH tonight and tomorrow night 6-9pm
- Tania OH tomorrow 2-4pm

- Journal Thursday
  - Carrizo: A High Performance, Energy Efficient 28 nm APU, pp 105 - 116