ESE 570: Digital Integrated Circuits and VLSI Fundamentals

Lec 19: March 30, 2017

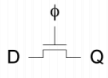
Dynamic Logic, Charge Injection

Lecture Outline

- Review: Sequential MOS Logic
  - D-Latch
- Dynamic Logic
  - Domino Logic
- Charge Leakage
- Charge Sharing
- Domino Logic Design Considerations
- Logic Comparisons

Latch Design

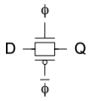
- Pass Transistor Latch
- Pros
  - + Tiny
  - + Low clock load
- Cons
  - – V_t drop
  - – nonrestoring
  - – backdriving
  - – output noise sensitivity
  - – dynamic
  - – diffusion input



Used in 1970's

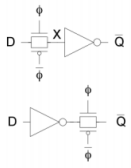
Latch Design

- **Transmission gate**
  - + **No V_t drop**
  - - **Requires inverted clock**



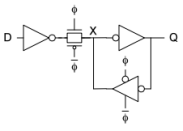
Latch Design

- Inverting buffer
  - + Restoring
  - + No backdriving
  - + Fixes either
    - Output noise sensitivity
    - Or diffusion input
  - – Inverted output



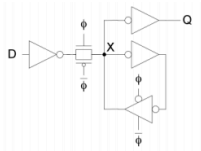
Latch Design

- **Buffered input**
  - + **Fixes diffusion input**
  - + **Noninverting**

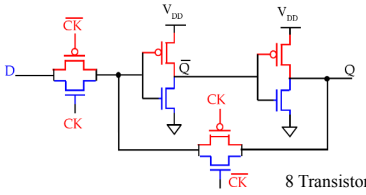


Typical Latch Design

- Buffered output
  - + No backdriving
- Widely used in standard cells
  - + Very robust (most important)
  - - Rather large
  - - Rather slow (1.5 – 2 FO4 delays)
  - - High clock loading

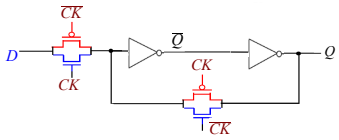


Static CMOS TG D-LATCH – 8 Transistors

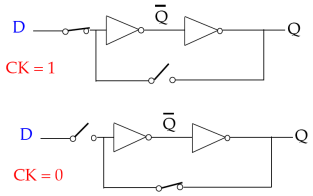


**Transistor level implementation using transmission gates requires fewer transistors

Static CMOS TG D-LATCH



Static CMOS TG D-LATCH

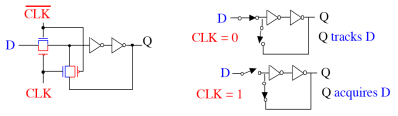


When CK = 1 output Q = D, and tracks D until CK = 0, the D-Latch is referred to positive level triggered.

When CK → 1 to 0, the Q = D is captured, held (or stored) in the Latch.

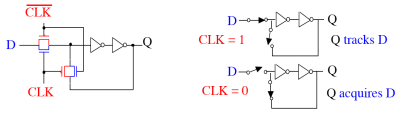
CMOS D Edge Triggered Flip-Flop

Negative D-Latch



NMOS
PMOS

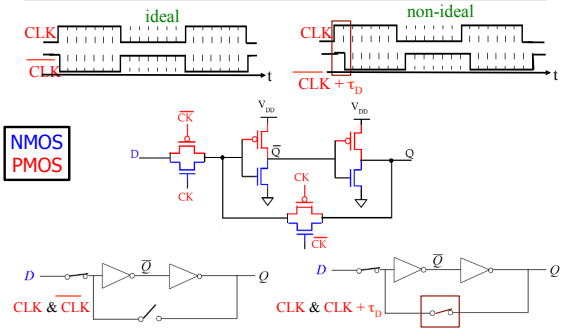
Positive D-Latch



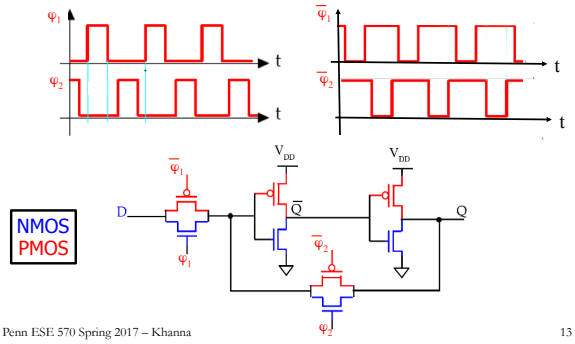
Positive Edge Triggered D Flip-Flop = Negative D-Latch + Positive D-Latch

Negative Edge Triggered D Flip-Flop = Positive D-Latch + Negative D-Latch

Impact of Non-ideal Clock on D-Latch Operation

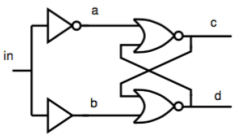


Two-Phase Clocked D-Latch (non-overlapping)



Non-overlapping Clocks

- Play with in Cadence
  - Will need for project



Dynamic Logic

Logic Comparison Overview

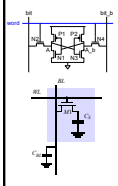
STATIC LOGIC GATES: valid logic levels are steady-state op points. Outputs are generated in response to input voltage levels after a certain time delay. Output levels are preserved as long as there is power, i.e. no refresh is needed.

DYNAMIC LOGIC GATES: valid logic level are not steady-state op points and depend on temporary storage of charge on parasitic node capacitances. Outputs are generated in response to input voltage levels and a clock. Requires periodic updating or refresh.

ADVANTAGES:

1. Allows implementation of simple sequential circuits with memory functions.
2. Use of common clock signals throughout the system enables the syncronization of various circuit blocks.
3. Implementation of complex functions genearlly use less die area than static circuits.
4. Often dissipates less dynamic power than static designs, due to smaller parasitic capacitances.

Logic Comparison Overview



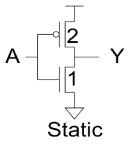
STATIC LOGIC GATES: valid logic levels are steady-state op points. Outputs are generated in response to input voltage levels after a certain time delay. Output levels are preserved as long as there is power, i.e. no refresh is needed.

DYNAMIC LOGIC GATES: valid logic level are not steady-state op points and depend on temporary storage of charge on parasitic node capacitances. Outputs are generated in response to input voltage levels and a clock. Requires periodic updating or refresh.

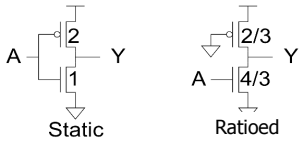
ADVANTAGES:

1. Allows implementation of simple sequential circuits with memory functions.
2. Use of common clock signals throughout the system enables the syncronization of various circuit blocks.
3. Implementation of complex functions genearlly use less die area than static circuits.
4. Often dissipates less dynamic power than static designs, due to smaller parasitic capacitances.

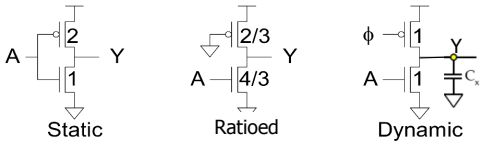
Comparison of Logic Implementations



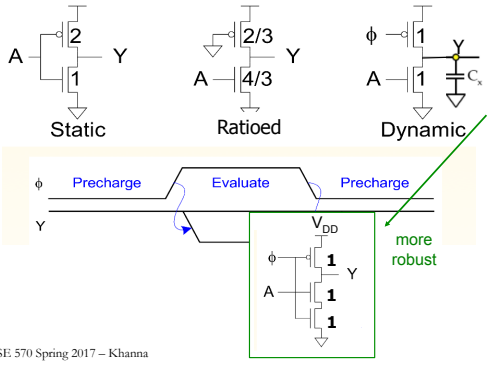
Comparison of Logic Implementations



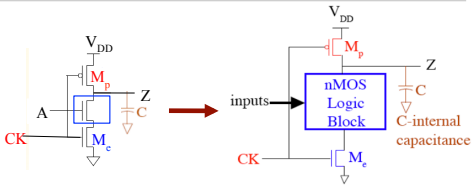
Comparison of Logic Implementations



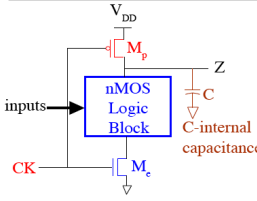
Comparison of Logic Implementations



Dynamic CMOS Precharge



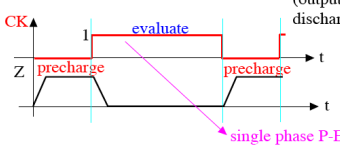
Dynamic CMOS Precharge



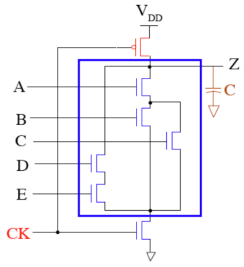
CK = 0 -> Z precharges to V_{DD} (inputs are applied, output is unavailable during precharge)

CK = 1 -> Z is selectively discharged to 0V or remains at V_{DD} (depends on logic values of inputs)

(output is only available after discharge of C is complete)



Dynamic (Clocked) Logic: Example



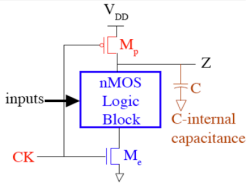
CK = 0 => Z = ?

CK = 1 => Z = ?

Comparison of Static and Dynamic Logic

ADVANTAGES ?

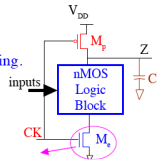
DISADVANTAGES ?



Comparison of Static and Dynamic Logic

ADVANTAGES

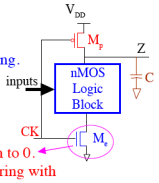
1. Requires N +2 transistors to realize an N-input gate.
2. Low static power dissipation.
3. No dc current paths to place constraints on device sizing.
4. Input capacitance same as pseudo nMOS gate.
5. Pull-up time is improved by active switch to V_{DD}.



Comparison of Static and Dynamic Logic

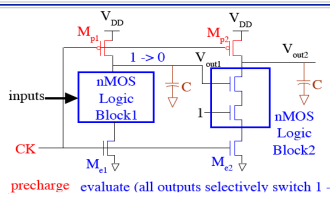
ADVANTAGES/DISADVANTAGES

1. Requires N +2 transistors to realize an N-input gate.
2. Low static power dissipation.
3. No dc current paths to place constraints on device sizing.
4. Input capacitance same as pseudo nMOS gate.
5. Pull-up time is improved by active switch to V_{DD}.

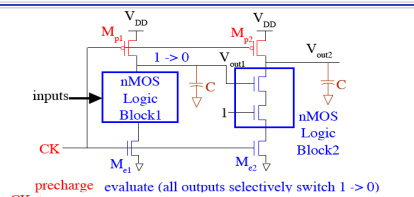


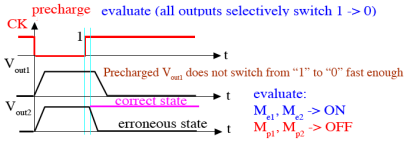
1. Output is available ≤ 50 % of the time.
2. Pull-down time is degraded due to series active switch to 0 .
3. Logic output value can be degraded due to charge sharing with other gate capacitances connected to the output.
4. Minimum clock rate determined by leakage on C.
5. Maximum clock rate determined by C discharge time and input delays.
6. Inputs can only change during the precharge phase. Inputs must be stable during evaluation; otherwise an incorrect value on an input could erroneously discharge the output node.

Cascaded Dynamic Logic



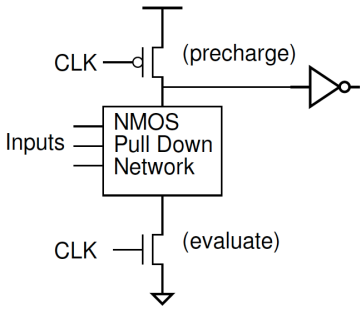
Cascaded Dynamic Logic





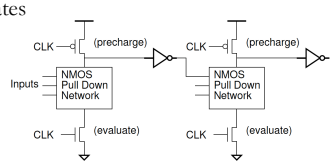
PROBLEM: ALL STAGES MUST EVALUATE SIMULTANEOUSLY
SINGLE CLOCK DOES NOT PERMIT PIPELINING OF STAGES

Domino Logic

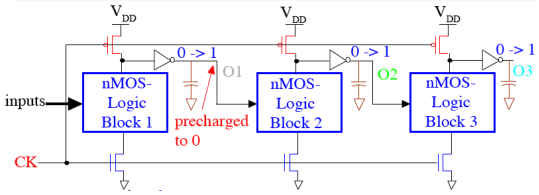


Requirements

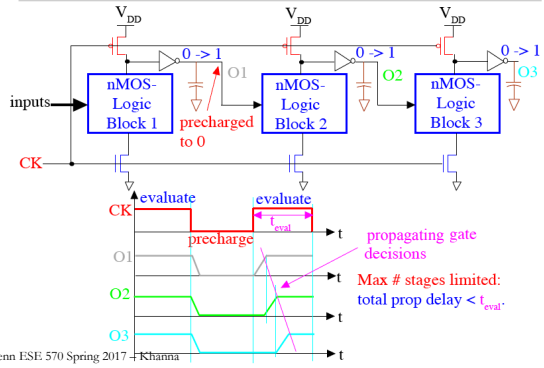
- Single transition
  - Once transitioned, it is done → like domino falling
- All inputs at 0 during precharge
  - 'Outputs' pre-charged to 1 then inverted to 0
    - I.e. Inputs are pre-charge to 0
- Non-inverting gates



Cascaded Domino CMOS Logic Gates

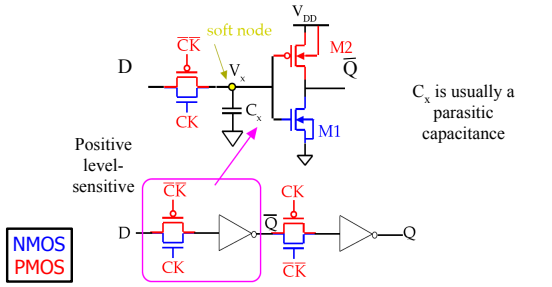


Cascaded Domino CMOS Logic Gates

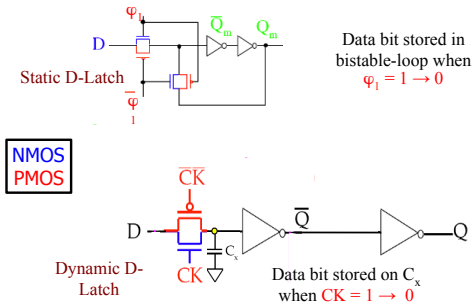


Charge Leakage

CMOS Dynamic D Latch

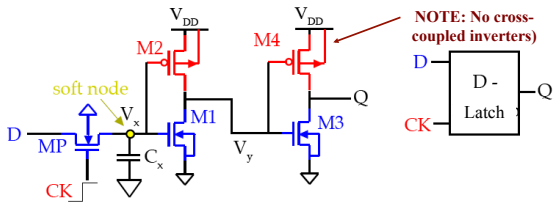


Comparison CMOS Static & Dynamic D-Latch



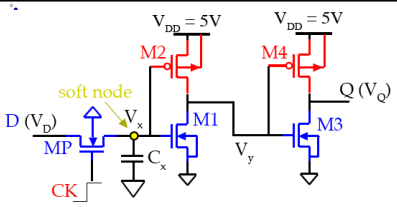
EXAMPLE:

Consider the following CMOS D Latch circuit:



CK = 1: MP turns ON. C_x is charged up or down through MP depending on the input D voltage level. Q = D.

CK = 0: MP turns OFF, and C_x is isolated from input D. Q is determined by charge stored on C_x during previous CK = 1.

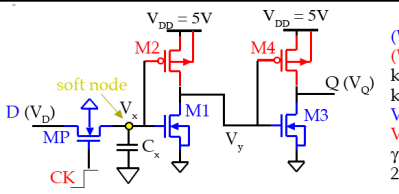


$(W/L)_n = 2$
$(W/L)_p = 4$
$k_n' = 20\ \mu A/V^2$
$k_p' = 10\ \mu A/V^2$
$V_{T0n} = 1.0\ V$
$V_{T0p} = -1.0\ V$
$\gamma = 0.37\ V^{1/2}$
$2\phi_F = -0.6\ V$

During CK = 1: Let D = 1, i.e. $V_D = V_{DD}$. MP is conducting and charges C_x to a "weak 1" (i.e. $V_x = V_{DD} - V_{TnMP}$). M1 is ON: $V_y = 0\ V < V_{T0nM3}$ => M3 is OFF: $V_Q = V_{DD} = 5\ V$ or Q = 1.

During CK = 0: Logic-level V_x is preserved through charge storage on C_x. However, V_x starts to drop due to leakage.

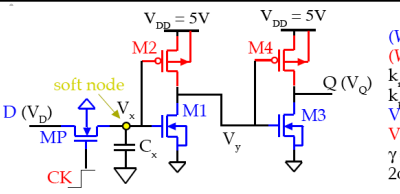
WHAT IS THE MINIMUM V_x NEEDED TO KEEP Q = 1 WHEN CK = 0?



$(W/L)_n = 2$
$(W/L)_p = 4$
$k_n' = 20\ \mu A/V^2$
$k_p' = 10\ \mu A/V^2$
$V_{T0n} = 1.0\ V$
$V_{T0p} = -1.0\ V$
$\gamma = 0.37\ V^{1/2}$
$2\phi_F = -0.6\ V$

NOTE: for $V_Q = V_{DD}$, M3 must be OFF => $V_y \le V_{T0n,M3} = 1.0\ V$; i.e. M1 is in LIN region and M2 is OFF

Assume that $V_y = V_{T0n} = 1V$, i.e. just small enough to keep M3 OFF => M1 LINEAR and M2 SATURATION ($V_{GD} > V_{T0p}$)



$(W/L)_n = 2$
$(W/L)_p = 4$
$k_n' = 20\ \mu A/V^2$
$k_p' = 10\ \mu A/V^2$
$V_{T0n} = 1.0\ V$
$V_{T0p} = -1.0\ V$
$\gamma = 0.37\ V^{1/2}$
$2\phi_F = -0.6\ V$

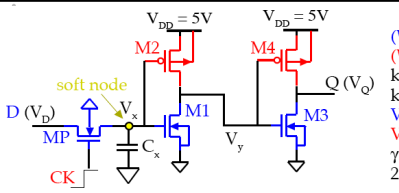
NOTE: for $V_Q = V_{DD}$, M3 must be OFF => $V_y \le V_{T0n,M3} = 1.0\ V$; i.e. M1 is in LIN region and M2 is OFF

Assume that $V_y = V_{T0n} = 1V$, i.e. just small enough to keep M3 OFF => M1 LINEAR and M2 SATURATION ($V_{GD} > V_{T0p}$)

$$\frac{k'_{n,M1}}{2}\left(\frac{W}{L}\right)_n\left[2(V_x - V_{T0n})V_y - V_y^2\right] = \frac{k_{P,M2}}{2}\left(\frac{W}{L}\right)_p(V_x - V_{DD} - V_{T0p})^2$$

$$\frac{20\mu A/V^2}{2}(2)\left[2(V_x - 1V)1V - 1V^2\right] = \frac{10\mu A/V^2}{2}(4)(V_x - 5V - (-1V))^2$$

$$\left[2V_x * 1V - 3V^2\right] = (V_x - 4V)^2 \Rightarrow V_x^2 - 10VV_x + 19V^2 = 0 \Rightarrow V_x = 2.55V$$



$(W/L)_n = 2$
$(W/L)_p = 4$
$k_n' = 20\ \mu A/V^2$
$k_p' = 10\ \mu A/V^2$
$V_{T0n} = 1.0\ V$
$V_{T0p} = -1.0\ V$
$\gamma = 0.37\ V^{1/2}$
$2\phi_F = -0.6\ V$

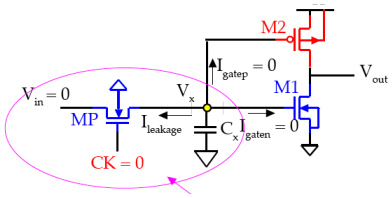
NOTE: for $V_Q = V_{DD}$, M3 must be OFF => $V_y \le V_{T0n,M3} = 1.0\ V$; i.e. M1 is in LIN region and M2 is OFF

Assume that $V_y = V_{T0n} = 1V$, i.e. just small enough to keep M3 OFF => M1 LINEAR and M2 SATURATION ($V_{GD} > V_{T0p}$)

$V_x = 2.55V$

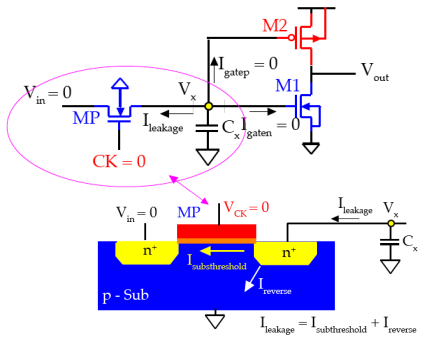
i.e. V_x can drop from $V_{x\text{-}max} = V_{DD} - V_{TMP}$ to $V_{x\text{-}min} = 2.55\ V$ due to charge leakage before V_Q is effected (i.e. the output changes state).

Charge Storage and Leakage

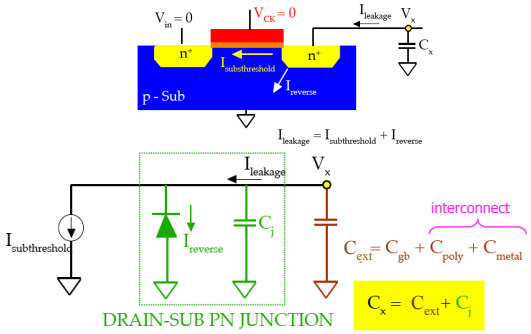


- Assume logic-high is stored onto V_x during active phase (CK=1)
- When CK=0, $V_{in} \rightarrow 0$

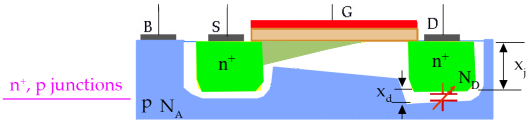
Charge Storage and Leakage



Charge Storage and Leakage



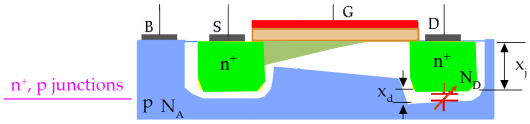
Reminder: (Bottom) Junction Capacitance



$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(\phi_0 + V)}$$ ↔ V = Ext Bias --> V_{SB}, V_{DB}

$$\phi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$ built-in junction potential

Reminder (Bottom) Junction Capacitance



$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(\phi_0 + V)}$$ ↔ V = Ext Bias --> V_{SB}, V_{DB}

$$\phi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$ built-in junction potential

$$C_{j0} = \frac{\varepsilon_{si}}{x_d} = \sqrt{\frac{\varepsilon_{si} q}{2}\cdot\frac{N_A\cdot N_D}{N_A+N_D}\cdot\frac{1}{\phi_0}}$$ Zero-bias capacitance (F/cm²)

Reminder Sidewall Junction Capacitance

n⁺, p⁺ junctions (Sidewalls)

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{si} q}{2}\cdot\frac{N_A(sw)\cdot N_D}{N_A(sw)+N_D}\cdot\frac{1}{\phi_0}}$$ (F/cm²)

Since all sidewalls have depth = x_j:

$C_{jsw} = C_{j0sw}\, x_j$ (F/cm)

Junction Capacitance

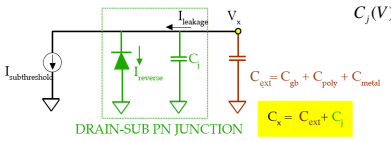
$$C_{j0} = \frac{\varepsilon_{si}}{x_d} = \sqrt{\frac{\varepsilon_{si} q}{2}\cdot\frac{N_A\cdot N_D}{N_A+N_D}\cdot\frac{1}{\phi_0}}$$

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{si} q}{2}\cdot\frac{N_A(sw)\cdot N_D}{N_A(sw)+N_D}\cdot\frac{1}{\phi_0}}$$

$$C_j(V) = \frac{A\cdot C_{j0}}{\sqrt{1+\frac{|V|}{\phi_0}}} + \frac{P\cdot C_{j0sw}}{\sqrt{1+\frac{|V|}{\phi_{0sw}}}}$$

Derived from 3.6 in text (p. 156-158)

Junction Capacitance



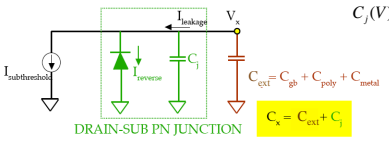
$$C_j(V) = \frac{A \cdot C_{j0}}{\sqrt{1+\frac{|V|}{\phi_0}}} + \frac{P \cdot C_{j0sw}}{\sqrt{1+\frac{|V|}{\phi_{0sw}}}}$$

$C_{ext} = C_{gb} + C_{poly} + C_{metal}$

$C_x = C_{ext} + C_j$

$$I_{leakage} = C_x \frac{dV_x}{dt}$$

Junction Capacitance



$$C_j(V) = \frac{A \cdot C_{j0}}{\sqrt{1+\frac{|V|}{\phi_0}}} + \frac{P \cdot C_{j0sw}}{\sqrt{1+\frac{|V|}{\phi_{0sw}}}}$$

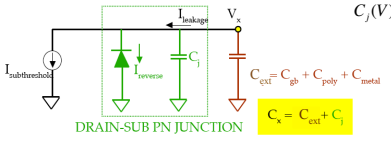
$C_{ext} = C_{gb} + C_{poly} + C_{metal}$

$C_x = C_{ext} + C_j$

$$I_{leakage} = C_x \frac{dV_x}{dt}$$

FOR QUICK ESTIMATE OF WORST CASE LEAKAGE BEHAVIOR
worst case hold time (t_{hold}) -> shortest time for V_x to drop from its initial logic "1" value $V_{x\text{-max}}$ to $V_{x\text{-min}}$ due to leakage.

Junction Capacitance



$$C_j(V) = \frac{A \cdot C_{j0}}{\sqrt{1+\frac{|V|}{\phi_0}}} + \frac{P \cdot C_{j0sw}}{\sqrt{1+\frac{|V|}{\phi_{0sw}}}}$$

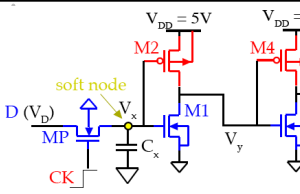
$C_{ext} = C_{gb} + C_{poly} + C_{metal}$

$C_x = C_{ext} + C_j$

$$I_{leakage} = C_x \frac{dV_x}{dt}$$

FOR QUICK ESTIMATE OF WORST CASE LEAKAGE BEHAVIOR
worst case hold time (t_{hold}) -> shortest time for V_x to drop from its initial logic "1" value $V_{x\text{-max}}$ to $V_{x\text{-min}}$ due to leakage.

$$\min(t_{hold}) = \Delta t = \frac{C_{x-min}}{I_{leakage-max}} \Delta V_x = \frac{C_{x-min}}{I_{leakage-max}} (V_{x-max} - V_{x-min})$$



$(W/L)_n = 2$
$(W/L)_p = 4$
$k_n' = 20\ \mu A/V^2$
$k_p' = 10\ \mu A/V^2$
$V_{T0n} = 1.0\ V$
$V_{T0p} = -1.0\ V$
$\gamma = 0.37\ V^{1/2}$
$2\phi_F = -0.6\ V$

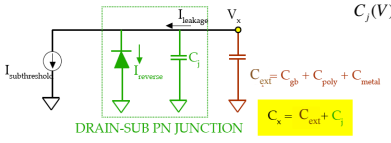
NOTE: for $V_Q = V_{DD}$, M3 must be OFF => $V_y \le V_{T0n,M3} = 1.0$ V; i.e. M1 is in LIN region and M2 is OFF

Assume that $V_y = V_{T0n} = 1V$, i.e. just small enough to keep M3 OFF => M1 LINEAR and M2 SATURATION ($V_{GD} > V_{T0p}$)

$V_x = 2.55V$

i.e. V_x can drop from $V_{x\text{-max}} = V_{DD} - V_{Tn,MP}$ to $V_{x\text{-min}} = 2.55$ V due to charge leakage before V_Q is effected (i.e. the output changes state).

Junction Capacitance



$$C_j(V) = \frac{A \cdot C_{j0}}{\sqrt{1+\frac{|V|}{\phi_0}}} + \frac{P \cdot C_{j0sw}}{\sqrt{1+\frac{|V|}{\phi_{0sw}}}}$$

$C_{ext} = C_{gb} + C_{poly} + C_{metal}$

$C_x = C_{ext} + C_j$

$$I_{leakage} = C_x \frac{dV_x}{dt}$$

FOR QUICK EXTIMATE OF WORST CASE LEAKAGE BEHAVIOR
worst case hold time (t_{hold}) -> shortest time for V_x to drop from its initial logic "1" value $V_{x\text{-max}}$ to $V_{x\text{-min}}$ due to leakage.

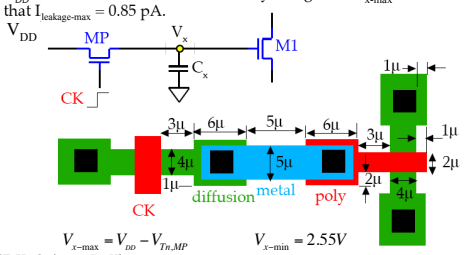
$$\min(t_{hold}) = \Delta t = \frac{C_{x-min}}{I_{leakage-max}} \Delta V_x = \frac{C_{x-min}}{I_{leakage-max}} (V_{x-max} - V_{x-min})$$

$V_{x-max} = V_{DD} - V_{Tn,MP}$ $\quad V_{x-min} = 2.55V$

$C_{x-min} = C_{ext} + C_{j,min} = C_{ext} + C_j(V = V_{x-max})$

Example

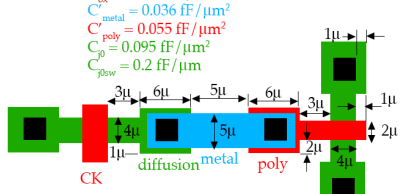
Consider the soft-node structure shown, which consists of the drain (or source depending on current direction) terminal of the pass transistor, connected to the poly gate of an nMOS driver transisitor via a metal interconnect. Estimate the worst-case holding time if $V_{DD} = 5$ V and the soft-node is initially charged to $V_{x\text{-max}}$. Assume that $I_{leakage\text{-max}} = 0.85$ pA.



$V_{x-max} = V_{DD} - V_{Tn,MP}$ $\quad V_{x-min} = 2.55V$

Example

$C_{ox} = 0.065\ fF/\mu m^2$
$C'_{metal} = 0.036\ fF/\mu m^2$
$C'_{poly} = 0.055\ fF/\mu m^2$
$C_{j0} = 0.095\ fF/\mu m^2$
$C_{j0sw} = 0.2\ fF/\mu m$



$C_{gb} = C_{ox}\ W\ L_{mask} = 0.065\ fF/\mu m^2\ (4\ \mu m \times 2\ \mu m) = 0.52\ fF$
$C_{metal} = C'_{metal}\ W\ L_{metal} = 0.036\ fF/\mu m^2\ (5\ \mu m \times 5\ \mu m) = 0.90\ fF$
$C_{poly} = C'_{poly}\ W\ L_{poly} = 0.055\ fF/\mu m^2\ (36\ \mu m^2 + 6\ \mu m^2 + 2\ \mu m^2) = 2.42\ fF$
$C_{n+p+} = CJSW\ P_{n+p+} = 0.200\ fF/\mu m\ (18\ \mu m + 6\ \mu m + 2\ \mu m) = 5.20\ fF$
$C_{n+p} = CJ\ A_{n+p} = 0.095\ fF/\mu m^2\ (36\ \mu m^2 + 12\ \mu m^2) = 4.56\ fF$

Example

$$\min(t_{hold}) = \Delta t = \frac{C_{x-\min}}{I_{leakage-\max}}\Delta V_x = \frac{C_{x-\min}}{I_{leakage-\max}}(V_{x-\max} - V_{x-\min})$$

$$C_{x-\min} = C_{ext} + C_{j,\min} = C_{ext} + C_j(V = V_{x-\max})$$

Example

$$\min(t_{hold}) = \Delta t = \frac{C_{x-\min}}{I_{leakage-\max}}\Delta V_x = \frac{C_{x-\min}}{I_{leakage-\max}}(V_{x-\max} - V_{x-\min})$$

VDD = 5.0 V
VT0 = 1.0 V
PB = 0.88 V
PBsw = 0.95 V
$I_{leakage,max} = 0.85\ pA$

$$C_{x-\min} = C_{ext} + C_{j,\min} = C_{ext} + C_j(V = V_{x-\max})$$

$$V_{x-\max} = V_{DD} - V_{Tn,MP} \approx 4V \qquad V_{x-\min} = 2.55V$$

Example

$$\min(t_{hold}) = \Delta t = \frac{C_{x-\min}}{I_{leakage-\max}}\Delta V_x = \frac{C_{x-\min}}{I_{leakage-\max}}(V_{x-\max} - V_{x-\min})$$

VDD = 5.0 V
VT0 = 1.0 V
PB = 0.88 V
PBsw = 0.95 V
$I_{leakage,max} = 0.85\ pA$

$$C_{x-\min} = C_{ext} + C_{j,\min} = C_{ext} + C_j(V = V_{x-\max})$$

$$V_{x-\max} = V_{DD} - V_{Tn,MP} \approx 4V \qquad V_{x-\min} = 2.55V$$

$$C_j(V) = \frac{A \cdot C_{j0}}{\sqrt{1 + \frac{|V|}{\phi_0}}} + \frac{P \cdot C_{j0sw}}{\sqrt{1 + \frac{|V|}{\phi_{0sw}}}}$$

$$C_j(V_{x-\max} = 4V) = \frac{4.56\,fF}{\sqrt{1 + \frac{|4V|}{0.88}}} + \frac{5.20\,fF}{\sqrt{1 + \frac{|4V|}{0.95}}} = 4.21\,fF$$

Example

$$\min(t_{hold}) = \Delta t = \frac{C_{x-\min}}{I_{leakage-\max}}\Delta V_x = \frac{C_{x-\min}}{I_{leakage-\max}}(V_{x-\max} - V_{x-\min})$$

VDD = 5.0 V
VT0 = 1.0 V
PB = 0.88 V
PBsw = 0.95 V
$I_{leakage,max} = 0.85\ pA$

$$C_{x-\min} = C_{ext} + C_{j,\min} = C_{ext} + C_j(V = V_{x-\max})$$

$$C_{x-\min} = 0.52\,fF + 0.90\,fF + 2.42\,fF + 4.21\,fF = 8.05\,fF$$

Example

$$\min(t_{hold}) = \Delta t = \frac{C_{x-\min}}{I_{leakage-\max}}\Delta V_x = \frac{C_{x-\min}}{I_{leakage-\max}}(V_{x-\max} - V_{x-\min})$$

VDD = 5.0 V
VT0 = 1.0 V
PB = 0.88 V
PBsw = 0.95 V
$I_{leakage,max} = 0.85\ pA$

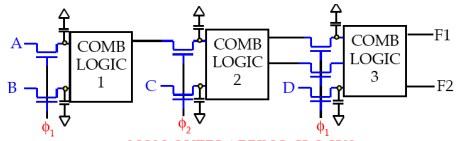
$$C_{x-\min} = C_{ext} + C_{j,\min} = C_{ext} + C_j(V = V_{x-\max})$$

$$C_{x-\min} = 0.52\,fF + 0.90\,fF + 2.42\,fF + 4.21\,fF = 8.05\,fF$$

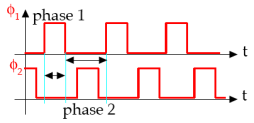
$$\min(t_{hold}) = \frac{8.05\,fF}{0.85\,pA}(4V - 2.55V) = 13.73\,ms$$

Charge Sharing

Dynamic Circuit Techniques



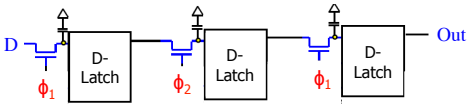
ϕ_1, ϕ_2 NON-OVERLAPPING CLOCKS



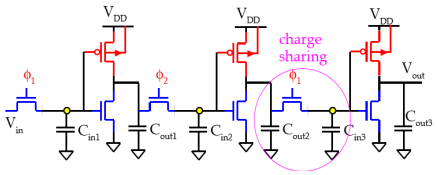
LOGIC LEVELS DURING INACTIVE CLOCK PHASE ARE STORED ON INPUT CAPS

Shift Register

- *Shift registers* store and delay data
- Simple design: cascade of latches



Shift Register with Dynamic D Latches



MAX CLOCK FREQUENCY IS DETERMINED BY SIGNAL PROPOGATION DELAY THROUGH ONE INVERTER STAGE.

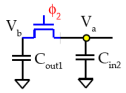
HIGH Portion of ϕ_1, ϕ_2 CLOCK PHASES MUST BE LONG ENOUGH:
C_{in} to charge up or down and C_{out} to charge to new value.

When $V_{out(i)}$ = 0V (or 5V) and $V_{in(i+1)}$ = 5V (or 0V) for i = 1,2 (stage)

"Charge Sharing" is an issue when φ_1/φ_2 close.

Charge Sharing

$V_b >> V_a$



CHARGE SHARING

$\phi_2 = 0$: $Q_{out1} = C_{out1} V_b$ and $Q_{in2} = C_{in2} V_a$

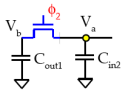
$\phi_2 = 1$: $Q_{total} = C_{out1} V_b + C_{in2} V_a$ and $C_{total} = C_{out1} + C_{in2}$

The resulting voltage across C_{total} is

$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1} V_b + C_{in2} V_a}{C_{out1} + C_{in2}}$$

Charge Sharing

$V_b >> V_a$



CHARGE SHARING

$\phi_2 = 0$: $Q_{out1} = C_{out1} V_b$ and $Q_{in2} = C_{in2} V_a$

$\phi_2 = 1$: $Q_{total} = C_{out1} V_b + C_{in2} V_a$ and $C_{total} = C_{out1} + C_{in2}$

The resulting voltage across C_{total} is

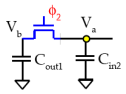
$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1} V_b + C_{in2} V_a}{C_{out1} + C_{in2}}$$

If $V_b = V_{DD}$ and $V_a << V_b$ => $V_R \approx \frac{C_{out1} V_{DD}}{C_{out1} + C_{in2}}$

$V_R \approx V_{DD}$ if $C_{out1} >> C_{in2}$

Charge Sharing

$V_b >> V_a$



CHARGE SHARING

"Rule of Thumb" make $C_{out1} = 10\ C_{in2}$

$\phi_2 = 0$: $Q_{out1} = C_{out1} V_b$ and $Q_{in2} = C_{in2} V_a$

$\phi_2 = 1$: $Q_{total} = C_{out1} V_b + C_{in2} V_a$ and $C_{total} = C_{out1} + C_{in2}$

The resulting voltage across C_{total} is

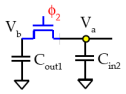
$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1} V_b + C_{in2} V_a}{C_{out1} + C_{in2}}$$

If $V_b = V_{DD}$ and $V_a << V_b$ => $V_R \approx \frac{C_{out1} V_{DD}}{C_{out1} + C_{in2}}$

$V_R \approx V_{DD}$ if $C_{out1} >> C_{in2}$

Charge Sharing

$V_b << V_a$



CHARGE SHARING

$\phi_2 = 0$: $Q_{out1} = C_{out1} V_b$ and $Q_{in2} = C_{in2} V_a$

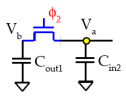
$\phi_2 = 1$: $Q_{total} = C_{out1} V_b + C_{in2} V_a$ and $C_{total} = C_{out1} + C_{in2}$

The resulting voltage across C_{total} is

$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1} V_b + C_{in2} V_a}{C_{out1} + C_{in2}}$$

Charge Sharing

$V_b << V_a$



CHARGE SHARING

$\phi_2 = 0$: $Q_{out1} = C_{out1} V_b$ and $Q_{in2} = C_{in2} V_a$

$\phi_2 = 1$: $Q_{total} = C_{out1} V_b + C_{in2} V_a$ and $C_{total} = C_{out1} + C_{in2}$

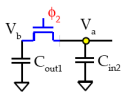
The resulting voltage across C_{total} is

$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1} V_b + C_{in2} V_a}{C_{out1} + C_{in2}}$$

If $V_b = 0$ and $V_a >> V_b$ → $V_R \approx \frac{C_{in2} V_{DD}}{C_{out1} + C_{in2}}$

Charge Sharing

$V_b << V_a$



CHARGE SHARING

$\phi_2 = 0$: $Q_{out1} = C_{out1} V_b$ and $Q_{in2} = C_{in2} V_a$

$\phi_2 = 1$: $Q_{total} = C_{out1} V_b + C_{in2} V_a$ and $C_{total} = C_{out1} + C_{in2}$

The resulting voltage across C_{total} is

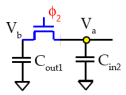
$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1} V_b + C_{in2} V_a}{C_{out1} + C_{in2}}$$

If $V_b = 0$ and $V_a >> V_b$ → $V_R \approx \frac{C_{in2} V_{DD}}{C_{out1} + C_{in2}}$

If $C_{out1} >> C_{in2}$ → $V_R \approx \frac{C_{in2} V_{DD}}{C_{out1}} << V_{DD}$

Charge Sharing

$V_b << V_a$



CHARGE SHARING

"Rule of Thumb" make $C_{out1} = 10\ C_{in2}$

$\phi_2 = 0$: $Q_{out1} = C_{out1} V_b$ and $Q_{in2} = C_{in2} V_a$

$\phi_2 = 1$: $Q_{total} = C_{out1} V_b + C_{in2} V_a$ and $C_{total} = C_{out1} + C_{in2}$

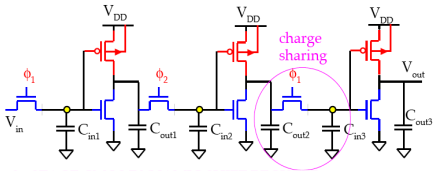
The resulting voltage across C_{total} is

$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_{out1} V_b + C_{in2} V_a}{C_{out1} + C_{in2}}$$

If $V_b = 0$ and $V_a >> V_b$ → $V_R \approx \frac{C_{in2} V_{DD}}{C_{out1} + C_{in2}}$

If $C_{out1} >> C_{in2}$ → $V_R \approx \frac{C_{in2} V_{DD}}{C_{out1}} << V_{DD}$

Shift Register with Dynamic D Latches



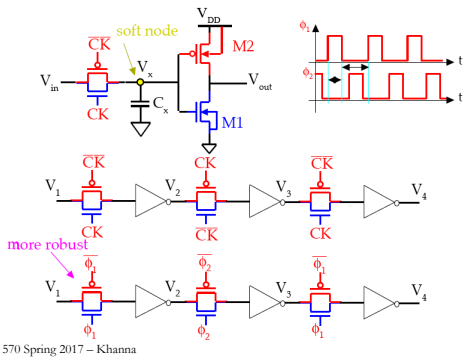
MAX CLOCK FREQUENCY IS DETERMINED BY SIGNAL PROPOGATION DELAY THROUGH ONE INVERTER STAGE.

HIGH Portion of ϕ_1, ϕ_2 CLOCK PHASES MUST BE LONG ENOUGH: C_{in} to charge up or down and C_{out} to charge to new value.

When $V_{out(i)}$ = 0V (or 5V) and $V_{in(i+1)}$ = 5V (or 0V) for i = 1,2 (stage)

"Charge Sharing" is an issue when φ_1, φ_2 close.

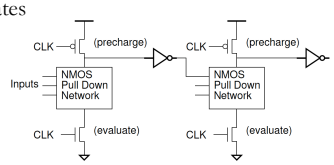
Shift Register with Dynamic D Latches



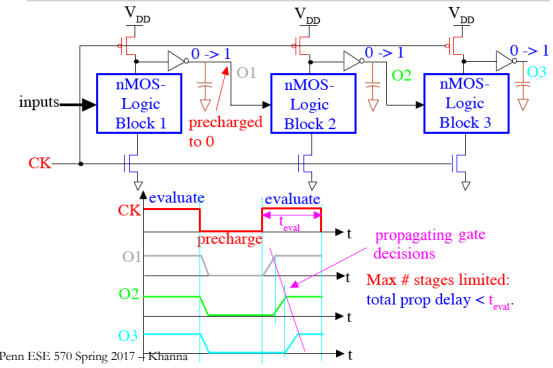
Domino Logic Design Considerations

Requirements

- Single transition
  - Once transitioned, it is done → like domino falling
- All inputs at 0 during precharge
  - 'Outputs' pre-charged to 1 then inverted to 0
    - I.e. Inputs are pre-charge to 0
- Non-inverting gates

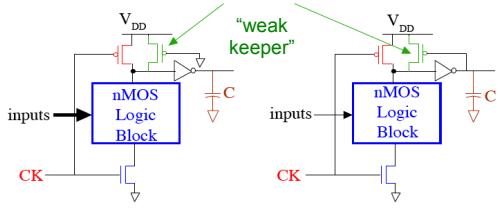


Cascaded Domino CMOS Logic Gates



Pre-charge Leakage

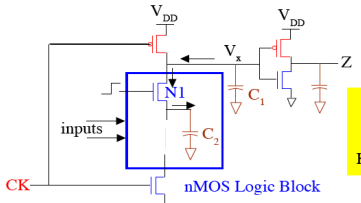
weak pull-up (small k_p, i.e. large L/W) pMOS transistor used maintain a precharged high if the clock were to stop. Weakened so that it does not interfere with pull-down



$(W/L)_{p\text{-keeper}} < (W/L)_{n\text{-min}}$

Also helps prevent erroneous discharges of C due to charge sharing with node capacitors within the nMOS Logic Block.

Charge Sharing within PDN

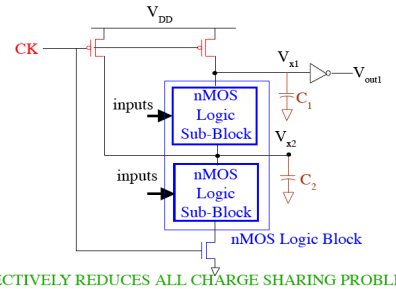


$V_x = \frac{V_{DD} C_1}{C_1 + C_2}$

KEEP $C_2 << C_1$

1. Assume initially that all inputs are 0V and voltage across C_2 is at 0V.
2. During pre-charge, i.e. CK = 0, C_1 is charged to V_{DD}.
3. If the input to N1 switches from 0 to 1 during the evaluation phase, i.e. CK = 1, charge initially stored on C_1 will be shared with C_2; thus, reducing the value of V_x.

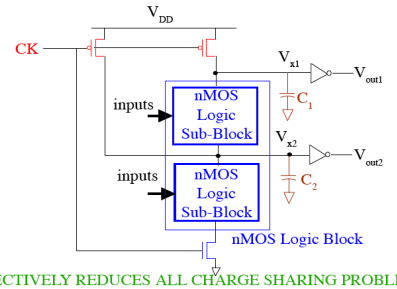
Charge Sharing within PDN



EFFECTIVELY REDUCES ALL CHARGE SHARING PROBLEMS DURING EVALUATION

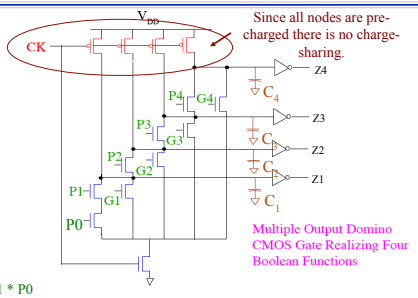
Charge Sharing within PDN

MULTIPLE OUTPUT DOMINO LOGIC - ALLOWS SIMULTANEOUS REALIZATION OF SEVERAL FUNCTIONS



EFFECTIVELY REDUCES ALL CHARGE SHARING PROBLEMS DURING EVALUATION

Charge Sharing within PDN



Z1 = G1 + P1 * P0
Z2 = G2 + P2 * G1 + P2 * P1 * P0 = G2 + P2 * Z1
Z3 = G3 + P3 * G2 + P3 * P2 * G1 + P3 * P2 * P1 * P0 = G3 + P3 * Z2
Z4 = G4 + P4 * G3 + P4 * P3 * G2 + P4 * P3 * P2 * G1 + P4 * P3 *P1 * P0 = G4 + P4 * Z3

CMOS Logic

- Best option in the majority of CMOS circuits
- Advantages:
  - Noise-immunity not sensitive to k_n/k_p
  - does not involve pre-charging of nodes
  - dissipates no DC power
  - layout can be automated
- Disadvantages:
  - Large fan-in gates lead to complex circuit structures (2N transistors)
  - larger parasitics
  - slower and higher dynamic power dissipation than alternatives
  - no clock and no synchronization.

Pseudo-nMOS/Ratioed Logic

- Finds widest utility in large fan-in gates
- Advantages:
  - Requires only N+1 transistors for N fan-in
  - smaller parasitics
  - faster and lower dynamic power dissipation than full CMOS
- Disadvantages:
  - Noise-immunity sensitive to k_n/k_p
  - dissipates DC power when pulled down
  - not well-suited for automated layout
  - no clock and no synchronization.

CMOS domino-logic

- Used for low-power, high-speed applications.
- Advantages:
  - Requires N+k transistors for N fan-in (size advantages of pseudo-nMOS)
  - dissipates no DC power
  - noise immunity not sensitive to k_n/k_p
  - use of clocks enables synchronous operation
- Disadvantages:
  - Relies on storage on soft nodes
  - will require thorough simulation at all the process corners to insure proper operation
  - some of the speed advantage over static gates is diminished by the required pre-charge (pre-discharge) time

Ideas

- Leads to clocked circuit discipline
  - Uses state holding element (eg. Latches and registers)
  - Prevents timing assumptions and complex reasoning about all possible timings
- Dynamic/clocked logic
  - Only build/drive one pulldown network
  - Fast transition propagation
- Domino Logic allows for cascading
- Charge Leakage
  - Constrains maximum clock frequency
- Charge Sharing with pass gates
  - Need to size carefully
- Different logic-types for different applications

Admin

- HW 7 out now
  - Due 4/6 @ midnight
  - EC due 4/9 @ midnight
- Start getting groups together for project
  - Groups of 2
  - Names due by 4/6
  - Use piazza to find partners