**University of Pennsylvania**
**Department of Electrical and System Engineering**
**Digital Integrated Cicruits AND VLSI Fundamentals**

ESE570, Spring 2019 HW 7: 4x4 Array Multiplier Friday, March 22

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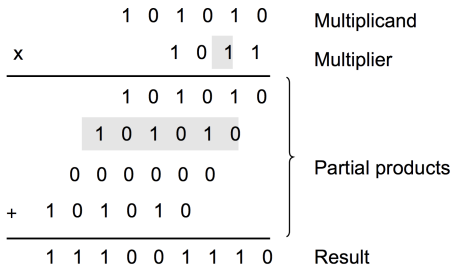
**Homework Due:** Friday April 5, 11:59PM

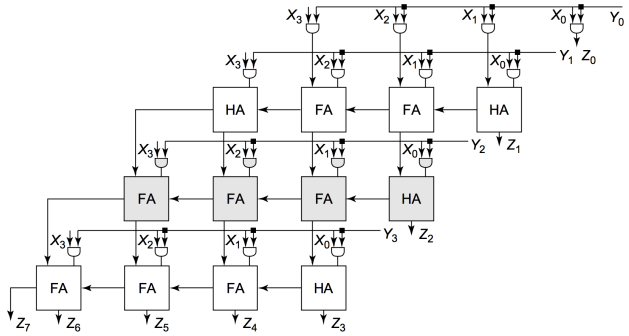
**Design Problem:** Design the circuit-level implementation of a full-adder bit-slice (for a 4x4 array multiplier).

- Your design will be completed in our .6u technology in Cadence
- Your design must be cascadable to build adders useable in multipliers.
- You must stay with a cascadable, bit-slice, design for this assignment.
- You may also design a half-adder (no Cin input) for use in the multiplier array for delay reduction. Nonetheless, the number of cell types needed should be a small constant number.

**Binary Multiplication:** Binary multiplication is done by doing additions. Partial products are calculated by multiplying the multiplicand by each bit of the multiplier and then summing the partial products. An example is shown below:




To implement the multiplication, you will design an array multiplier that multiplies two 4-bit inputs and calculates an 8-bit output. The array is shown below:



**Baseline Design:** You will create a design for your multiplier with all minimum sized devices and then modify your baseline into a delay-optimized design, which is discussed below.

- CMOS design: Use CMOS logic discipline, 5V= $V_{dd}$, and minimum size transistors.
- The design you implement must be measured with the following 3 design metrics:
  - *delay*: Measure the delay of a 4bx4b multiplication. This is the worst-case delay from two 4b inputs to all 8b of output. Load the outputs by the equivalent load as the input to your multiplier. Drive the inputs by the equivalent drive of one of your multipliers. You must consider what input case would give the worst case delay.
  - *active energy*: Measure the energy for the 4x4 multiplication in two cases:
    1. Maximum switching energy case (All inputs switch from $0 \rightarrow 1$)
    2. Average switching energy case (Half the inputs of each input switch from $0 \rightarrow 1$)
  - *leakage energy*: measure the leakage energy for one multiplier delay period when the inputs do not change in two cases:
    1. Maximum leakage energy case
    2. Minimum leakage energy case

    For leakage energy, the maximum and minimum case could vary depending on your implementation (eg. design of full adder, using a half adder, etc.). You should identify and justify your choice of inputs for each of the cases. (**Hint**: How many cases are there for each bit slice? How does the overall delay, leakage energy, or active energy compose from the results you get for a single bit slice?)
- With your homework, you should submit:
  - All schematics for your design, including test schematics
  - Description of operation of your design
  - Verified logical correctness of both your bit-slice(s) and array multiplier
  - Description of the input case for worst-case delay and why it gives the worst case delay.
  - Summary of the design metrics for design to two significant figures. Include supporting evidence in the form of equations and simulation results.

  **Hint:** Verify design in components. Test bit-slice before full multiplier.

**Optimized Design:** You will modify your Baseline Design into a delay-optimized design.

- You select gate structure, gate types, transistor sizes, and logic discipline.
- You may use any $V_{dd} \leq 5.0$V.
- Think about your list of issues/design-options to explore from the homework before you start detailed simulation to test your hypotheses and refine your designs. Determining the critical path for a 4x4 array multiplier is non-trivial since there are many identical length paths. Speeding up just one of them doesn't make sense and all critical paths must be optimized simultaneously.

- With your homework, you should submit:
  - All schematics for your optimized design, including test schematics
  - Verified logical correctness of both your bit-slice and array multiplier in the optimized design
  - Summary of the 3 design metrics (delay, active energy, and leakage energy)
  - A brief description of how you used the alternates and variations to arrive at the final design, highlighting what you learned from the designs. Include graphs and tables as appropriate to show how the alternatives compared and support your final design selection.
  - Table summary comparing your baseline and optimized design metrics