ESE 570: Digital Integrated Circuits and VLSI Fundamentals

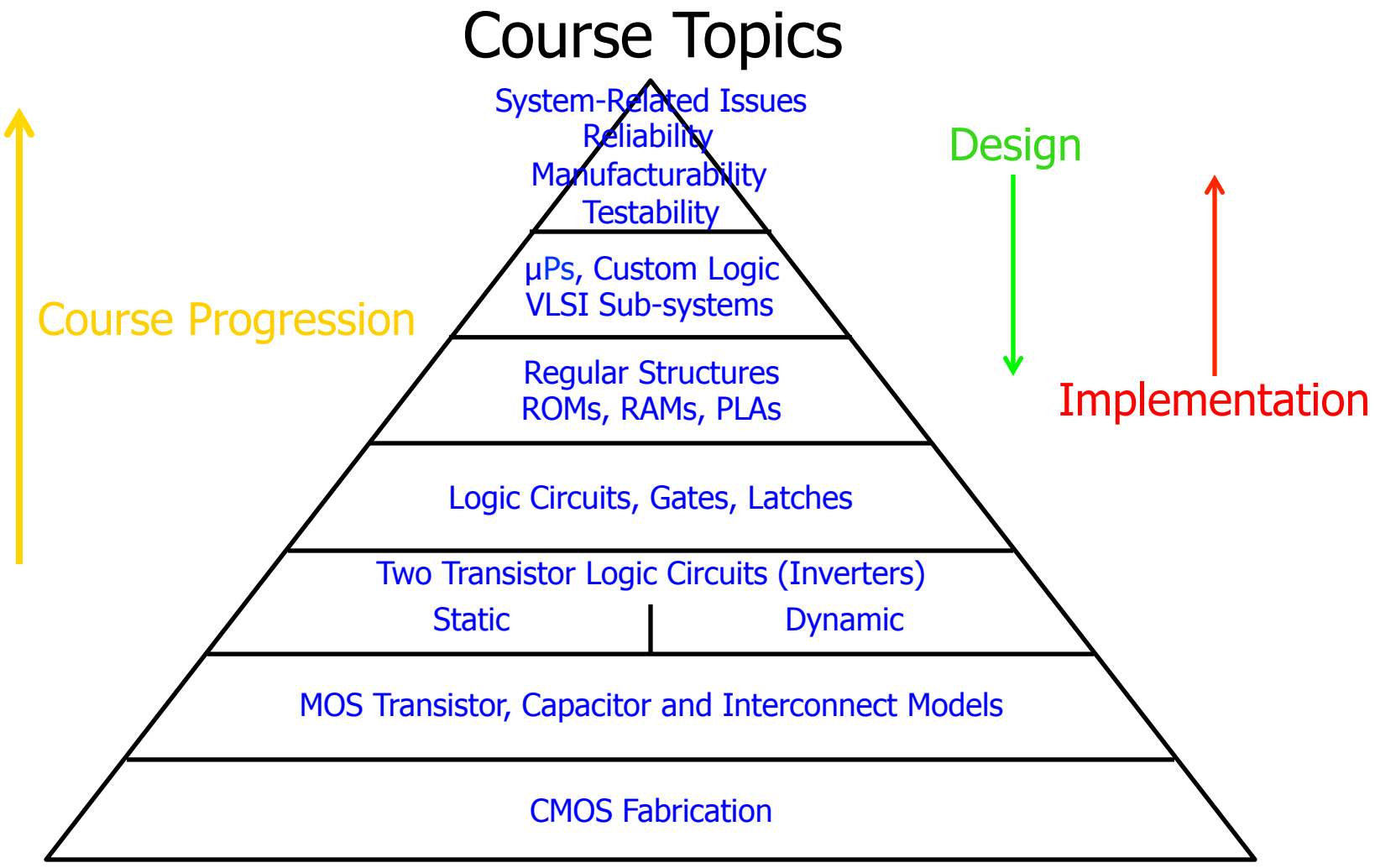
Lec 1: January 16, 2020

Introduction and Overview

Lecture Outline

- Course Topics Overview
- Learning Objectives
- Course Structure
- Course Policies
- Course Content
- Industry Trends
- Design Example

Course Topics Overview



Learning Objectives

- **Apply principles of hierarchical digital CMOS VLSI**, from the transistor up to the system level, to the understanding of CMOS circuits and systems that are suitable for CMOS fabrication.
- **Apply the models for state-of-the-art(ish) VLSI components**, fabrication steps, hierarchical design flow and semiconductor business economics to judge the manufacturability of a design and estimate its manufacturing costs.
- **Design digital circuits** that are manufacturable in CMOS.
- **Design simulated experiments using Cadence** to verify the integrity of a CMOS circuit and its layout.
- Apply the Cadence VLSI CAD tool suite **layout digital circuits for CMOS** fabrication and verify said circuits with layout parasitic elements.
- Apply course knowledge and the Cadence VLSI CAD tools in a team based **capstone design project** that involves much the same design flow they would encounter in a semiconductor design industrial setting. Capstone project is presented in a formal report due at the end of the semester.

Learning Objectives

- In other words…

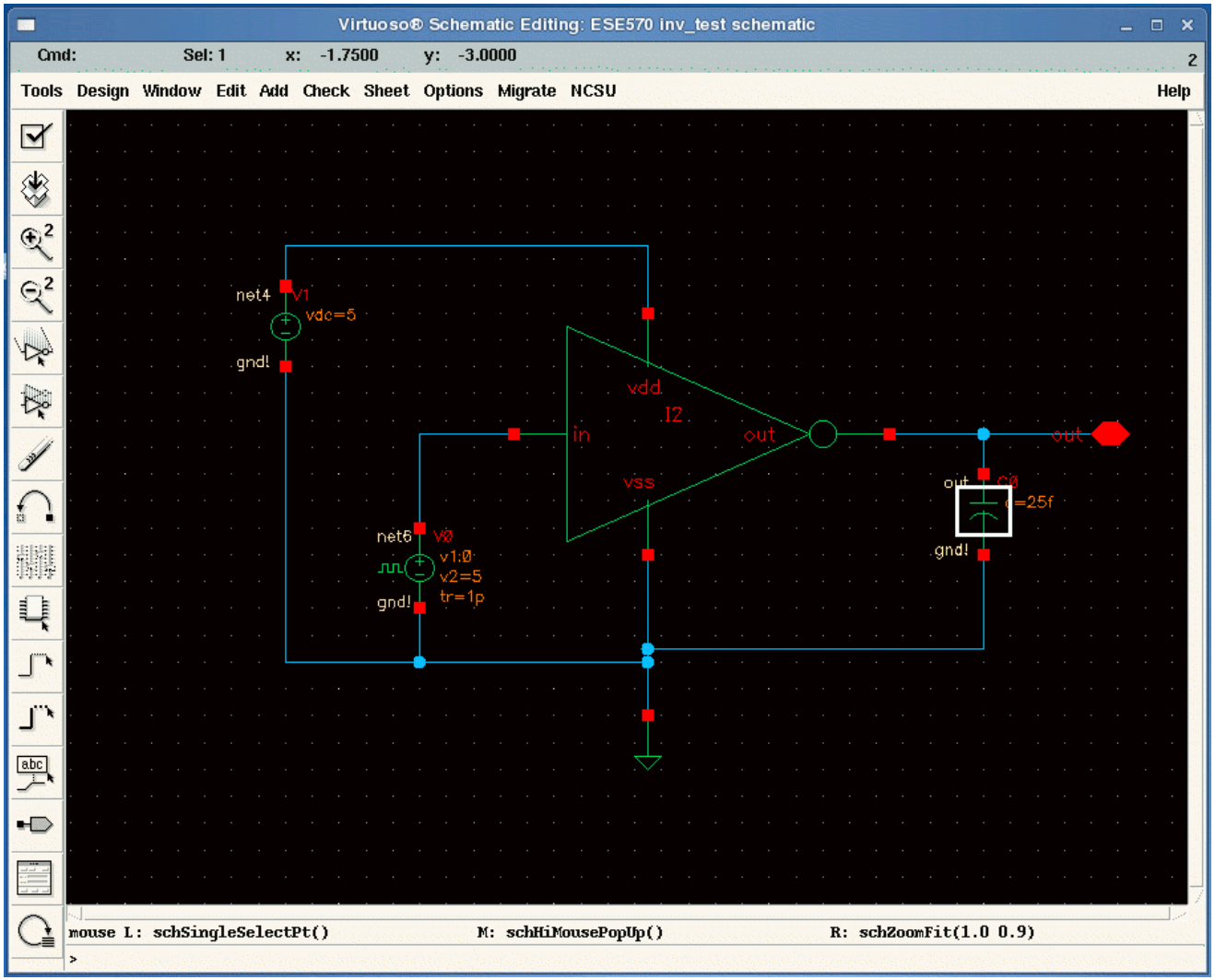
- Design in CADENCE*

*All the way to layout/manufacturability

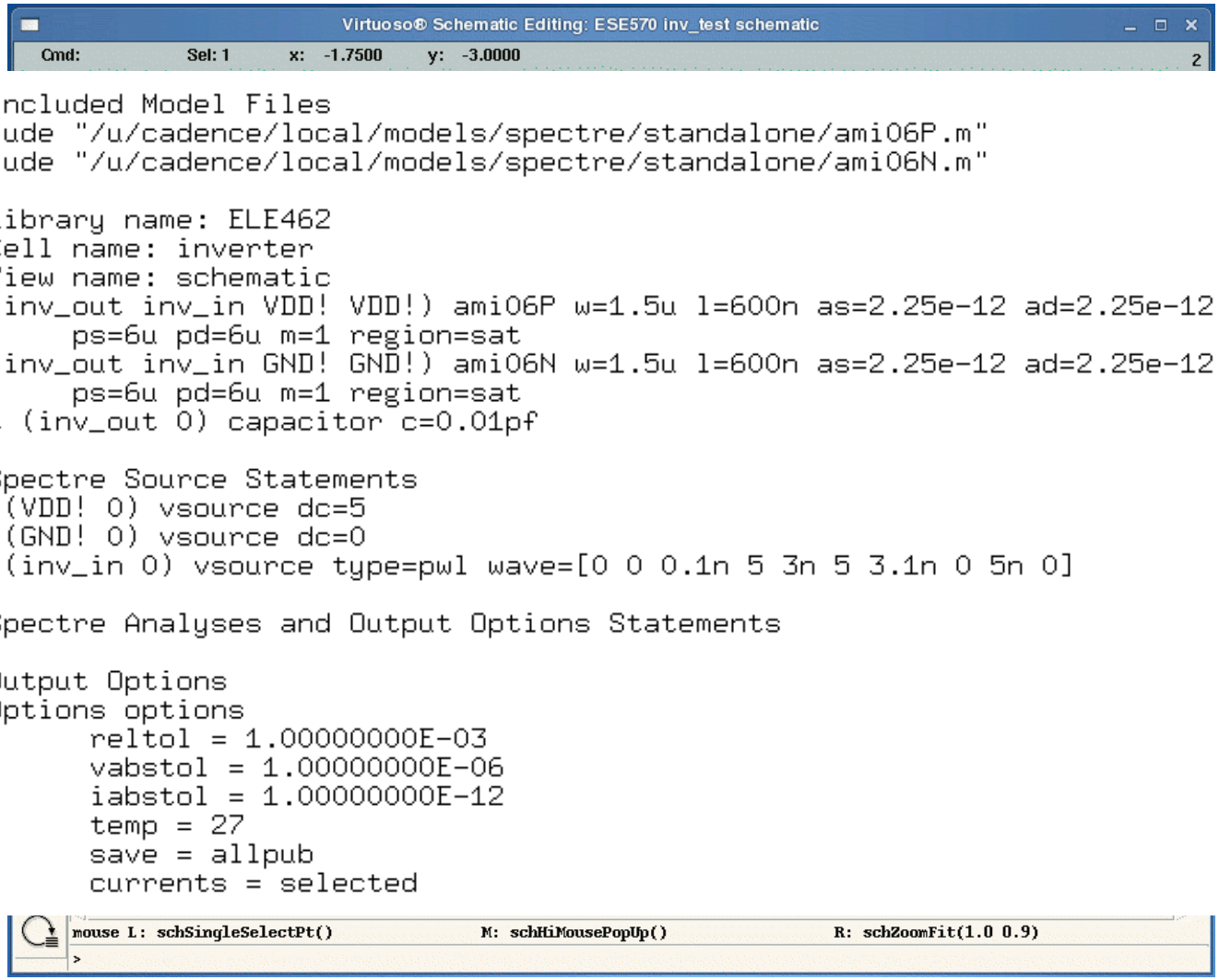
What is Cadence

- Industry standard CAD software for IC design
- Schematic capture
  - Create netlist (software code describing schematic)
- SPECTRE/SPICE simulator
  - Mathematical solver of differential equations describing fundamentals (Ex. KCL/KVL, Ohm's law, etc.)
- Design physical mask layers used for fabrication
- Extract parastics from physical layout for simulation

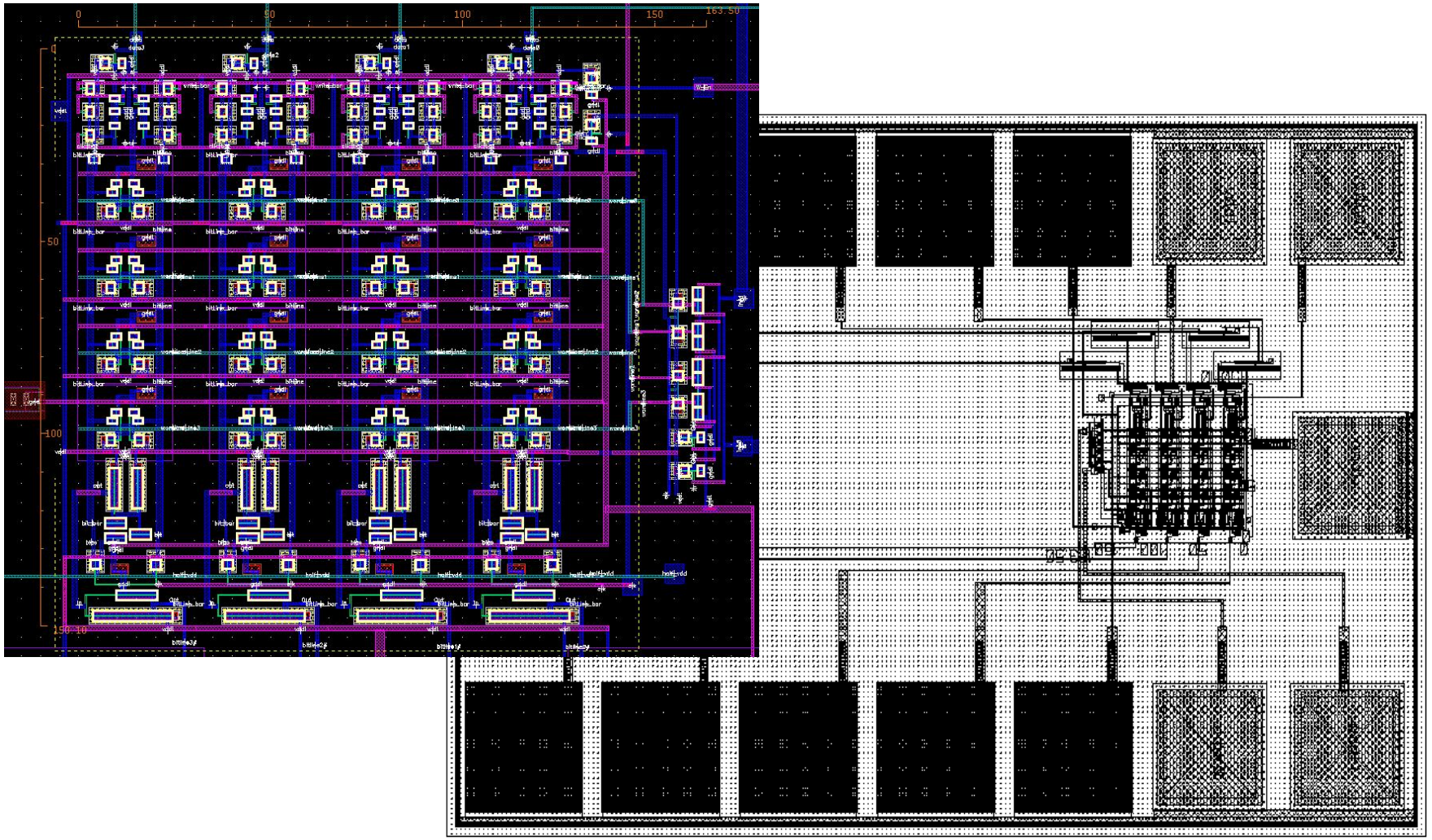
Schematic Capture



Schematic Capture



Layout in Cadence



Course Structure

- TR Lecture, 1:30-3:00pm in Towne 311
  - Start 5 minutes after, end 5 minutes early (~75-80min)
- Website (http://www.seas.upenn.edu/~ese570/)
  - Course calendar is used for all handouts (lectures slides, assignments, and readings)
  - Canvas used for assignment submission and grades
  - Piazza used for announcements and discussions

Course Structure

- Course Staff (complete info on course website)
- Instructor: Tania Khanna
  - Office hours – Wednesday 1-3 pm or by appointment
  - Email: taniak@seas.upenn.edu
    - Best way to reach me
- TAs:
  - Yuanlong Xiao, AJ Geers, Wes Sheker
    - Office hours: TBD

Course Structure

- Lectures
  - Statistically speaking, you will do better if you come to lecture
  - Better if interactive, **everyone** engaged
    - Asking and answering questions
    - Actively thinking about material
- Textbook
  - CMOS Digital Integrated Circuits Analysis and Design, Kang, Leblebici, and Kim, 4th edition
  - Class will follow text structure

Course Structure

- Cadence
  - Technology: AMI .6u C5N (3M, 2P, high-res)
    - Possibly updated to 15nm process*
  - Schematic simulation (SPECTRE simulator)
    - Design, analysis and test
  - Layout and verification
  - Analog extracted simulation
  - Verilog

Course Structure - Assignments/Exams

- Homework – 1-2 week(s) long (8 total) [25%]
  - Due Fridays at midnight
  - HW 1 out now
- Project – two+ weeks long [25%]
  - Design oriented
  - Project – design and layout digital memory
    - Propose alternate project
    - Propose extra credit to use your memory (eg. FIFO, shift reg, etc.)
- In class mini quizzes – 2 in class [5%]
  - 15 minutes at the beginning of class
- Midterm exam [20%]
- Final exam [25%]

Course Policies

See web page for full details

- Turn homework in Canvas
  - Anything handwritten/drawn must be clearly legible
  - Submit CAD generated figures, graphs, results when specified
  - NO LATE HOMEWORKS!
- Individual work (except project)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help

Course Content

- Introduction
- Fabrication
- MOS Transistor Theory and Models
- MOS Models and IV characteristics
- Inverters: Static Characteristics and Performance
- Inverters: Dynamic Characteristics and Performance
- Combinational Logic Types (CMOS, Ratioed, Pass) and Performance
- Sequential Logic
- Dynamic Logic
- VLSI design and Scaling
- Memory Design
- I/O Circuits and Inductive Noise
- CLK Generation
- Transmission Lines

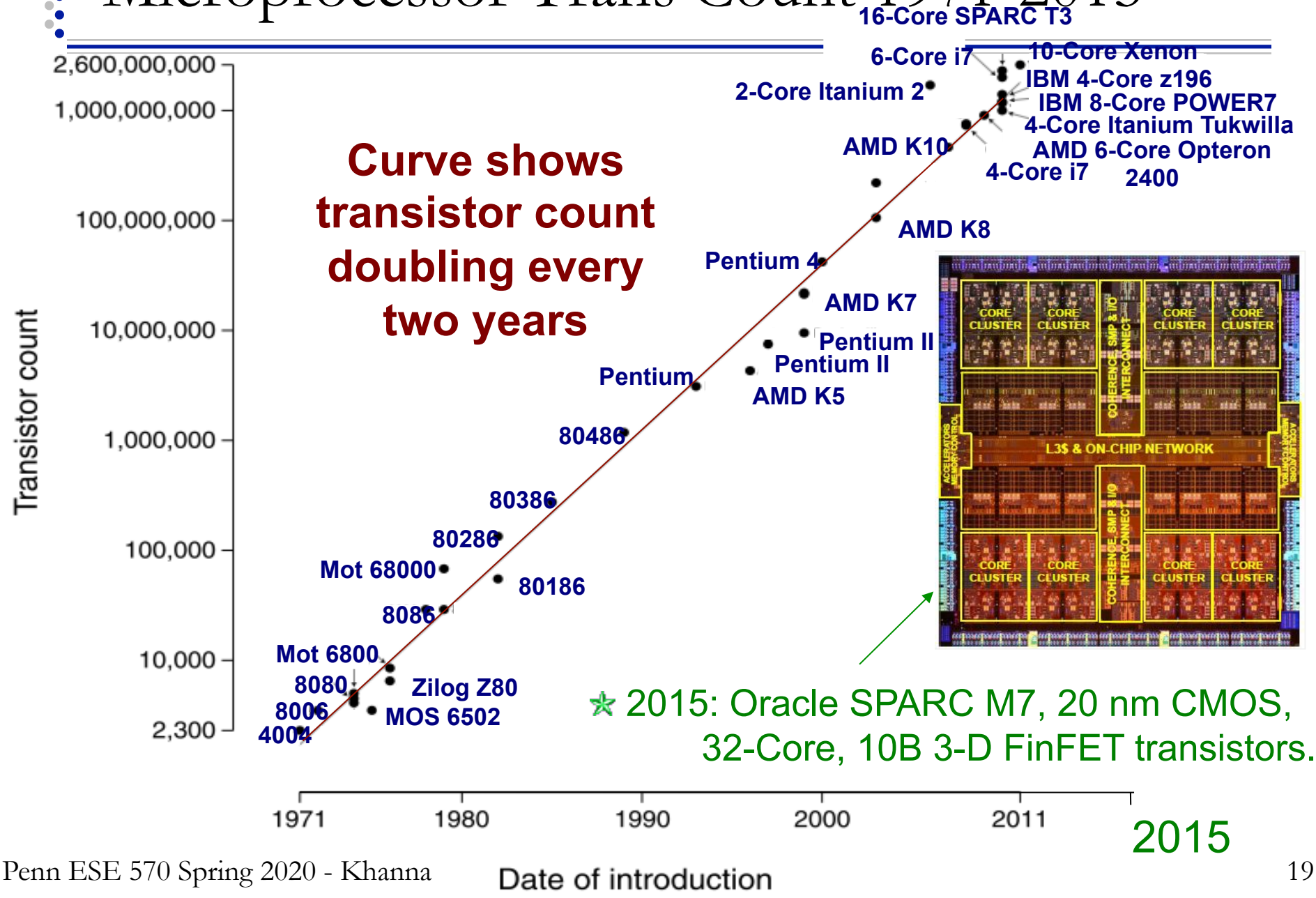
Course Content

ESE570 Spring 2020 Working Schedule

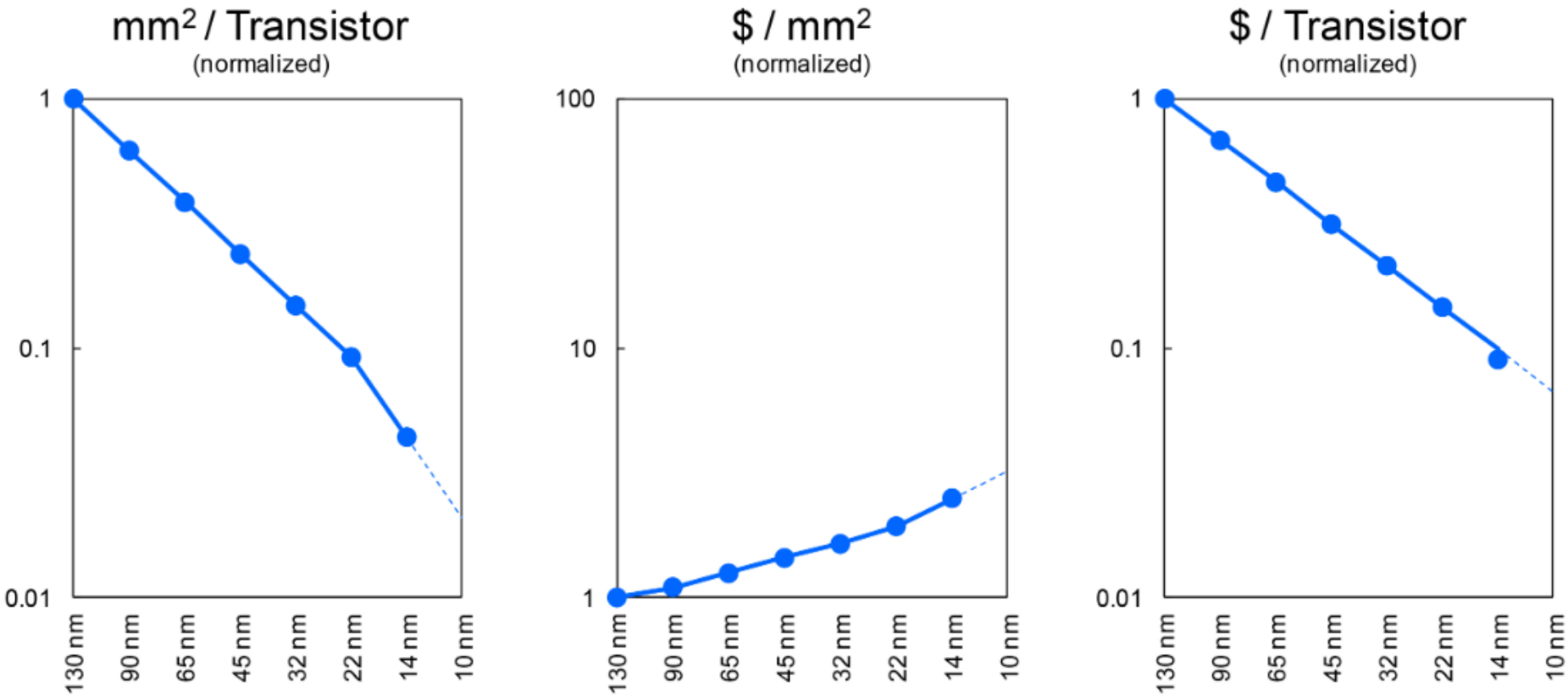
Wk	Lect.	Date		Lecture	Slides	Due	Reading
1	1	1/16	Th	Intro/Overview	[lec1] [lec1_6up]		1.1-1.3; review course webpage completely
2	2	1/21	T	MOS Fabrication pt. 1: Physics and Methodology			2.1-2.3, 3.5 (pp147-151)
	3	1/23	Th	MOS Fabrication pt. 2: Design Rules and Layout			2.5-2.6
		1/24	F			HW1 HW1.xls	
3	4	1/28	T	MOS Transistor Thoery, MOS Model			3.1, 3.3
	5	1/30	Th	MOS Operating Regions pt. 1			3.4-3.5
		1/31	F			HW 2	
4	6	2/4	T	MOS Operating Regions pt. 2			4.3-4.5
	7	2/6	Th	MOS SPICE models, MOS parasitic details			3.6
		2/7	F			HW 3	
5	8	2/11	T	MOS Inverters: Static Characteristics			5.1-5.2
	9	2/13	Th	MOS Inverters: Static Performance			5.4
		2/14	F			HW 4	
6	10	2/18	T	MOS Inverters: Dynamic Characteristics			6.1-6.3, 6.4
	11	2/20	Th	MOS Inverters: Dynamic Performance		Quiz 1	6.1-6.3, 6.4
7	12	2/25	T	Interconnect Delay			6.6
	13	2/27	Th	Combinational Logic: CMOS			7.3
		2/28	F			HW 5	
8	14	3/3	T	Combinational Logic: Ratioed and Pass Logic			7.2, 7.5, 9.1
	15	3/5	Th	Pass Logic (cont'd)		Quiz 2	7.5, 9.2
9		3/10	T	SPRING BREAK -- no class			
		3/12	Th	SPRING BREAK -- no class			
		3/15	Su			HW 6	
10	16	3/17	T	Static Logic roundup, and Euler Paths			6.7, 7.4
		3/19	Th	Midterm Exam, during class in TBD			
11	17	3/24	T	Energy Optimization, Design Space Exploration			6.6-6.7
	18	3/26	Th	Sequential MOS Logic and Timing Hazards			8.1-8.3, 8.5
	19	3/31	T	Timizing Hazards and Dynamic Logic			9.5-9.6

Industry Trends

Microprocessor Trans Count 1971-2015

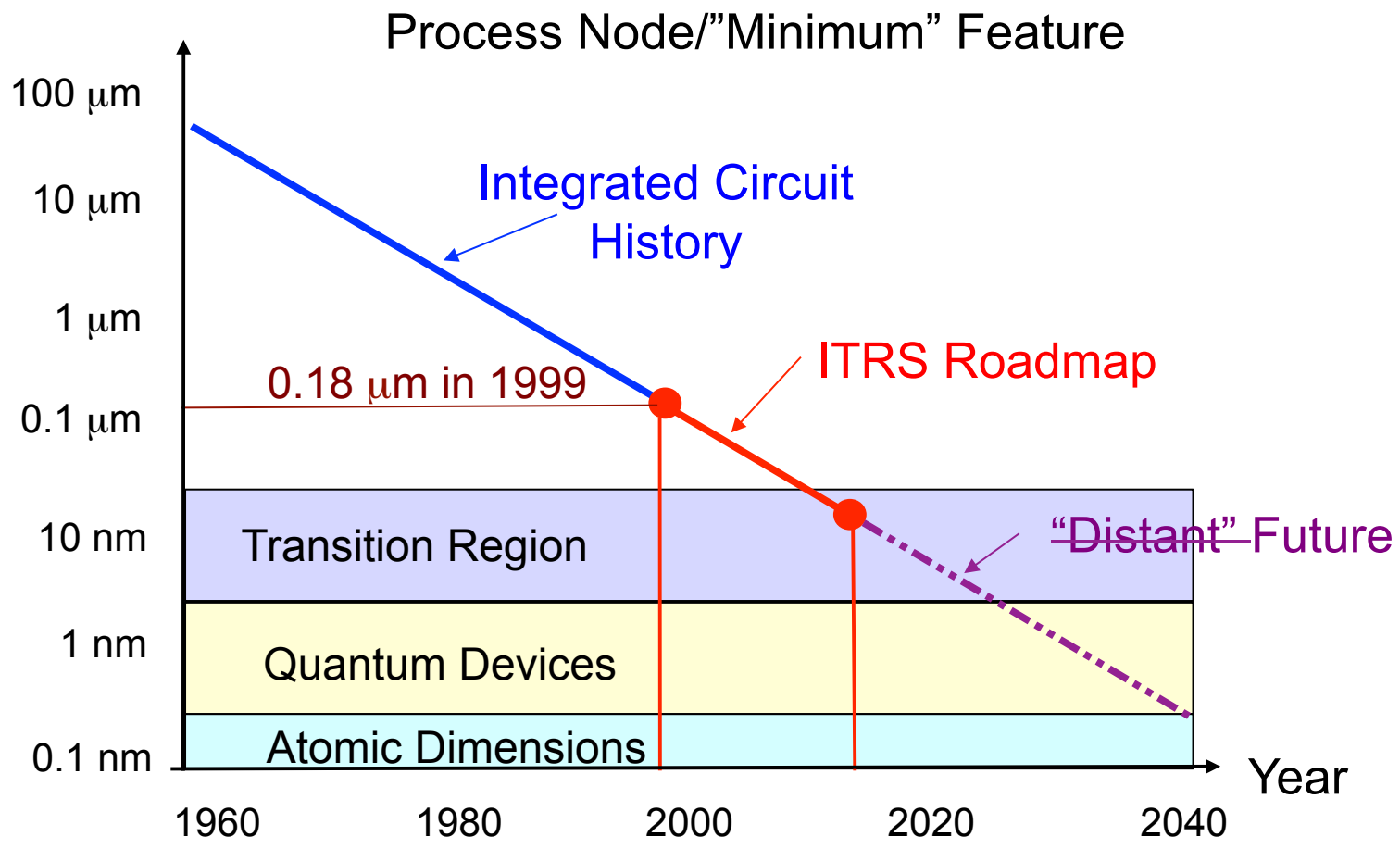


Intel Cost Scaling



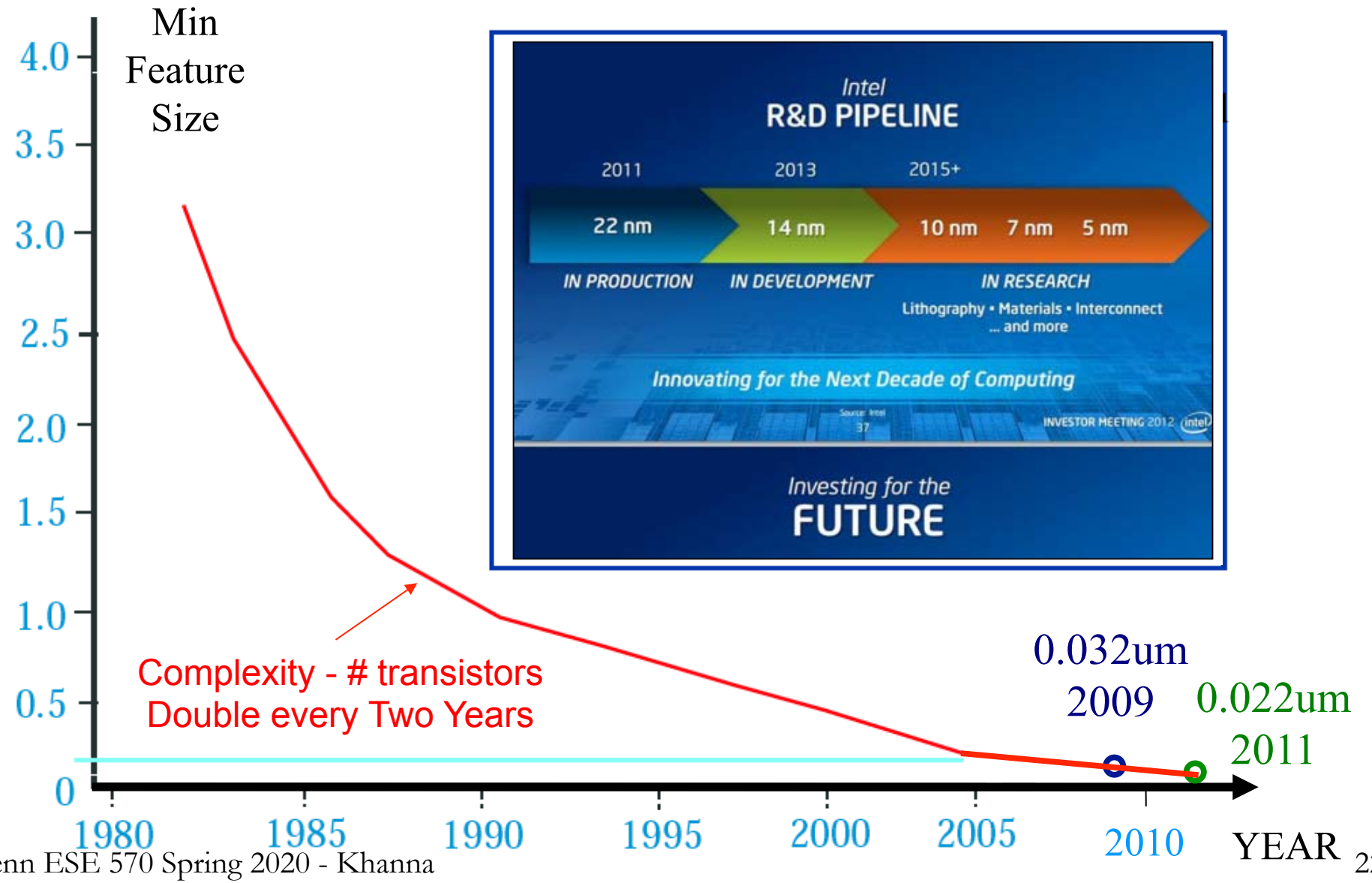
http://www.anandtech.com/show/8367/intels-14nm-technology-in-detail

Trend – "Minimum" Feature Size vs. Year



"Minimum" Feature Measure = line/gate conductor width or half-pitch (adjacent 1st metal layer lines or adjacent transistor gates)

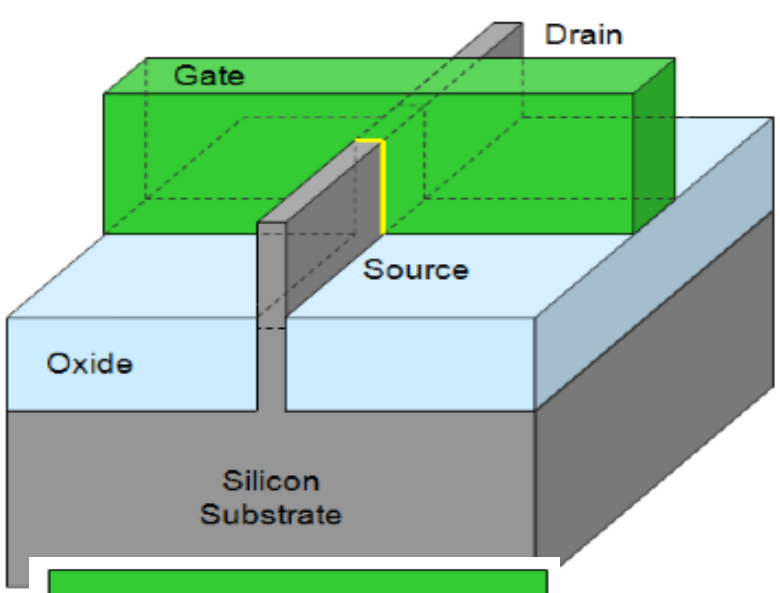
Moore's Law Impact on Intel uComputers

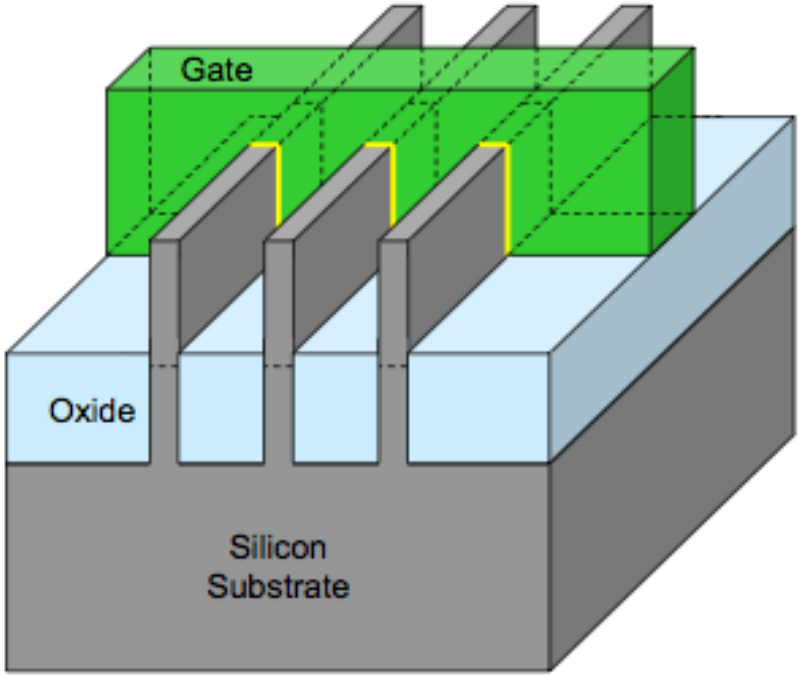


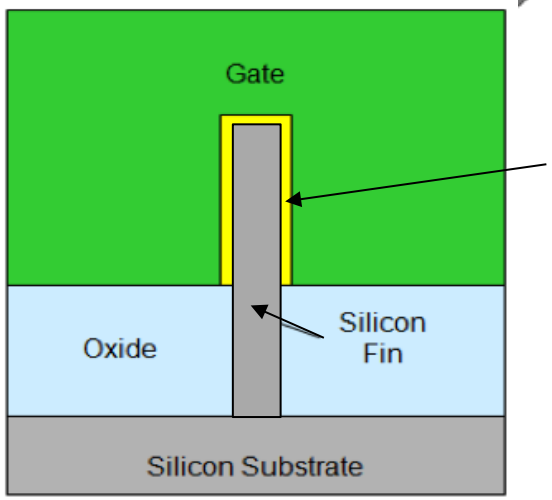
More Moore → Scaling

- Geometrical Scaling
  - continued shrinking of horizontal and vertical physical feature sizes
- Equivalent Scaling
  - 3-dimensional device structure improvements and new materials that affect the electrical performance of the chip even if no geometrical scaling
- Design Equivalent Scaling
  - design technologies that enable high performance, low power, high reliability, low cost, and high design productivity even if neither geometrical nor equivalent scaling can be used

22nm 3D FinFET Transistor







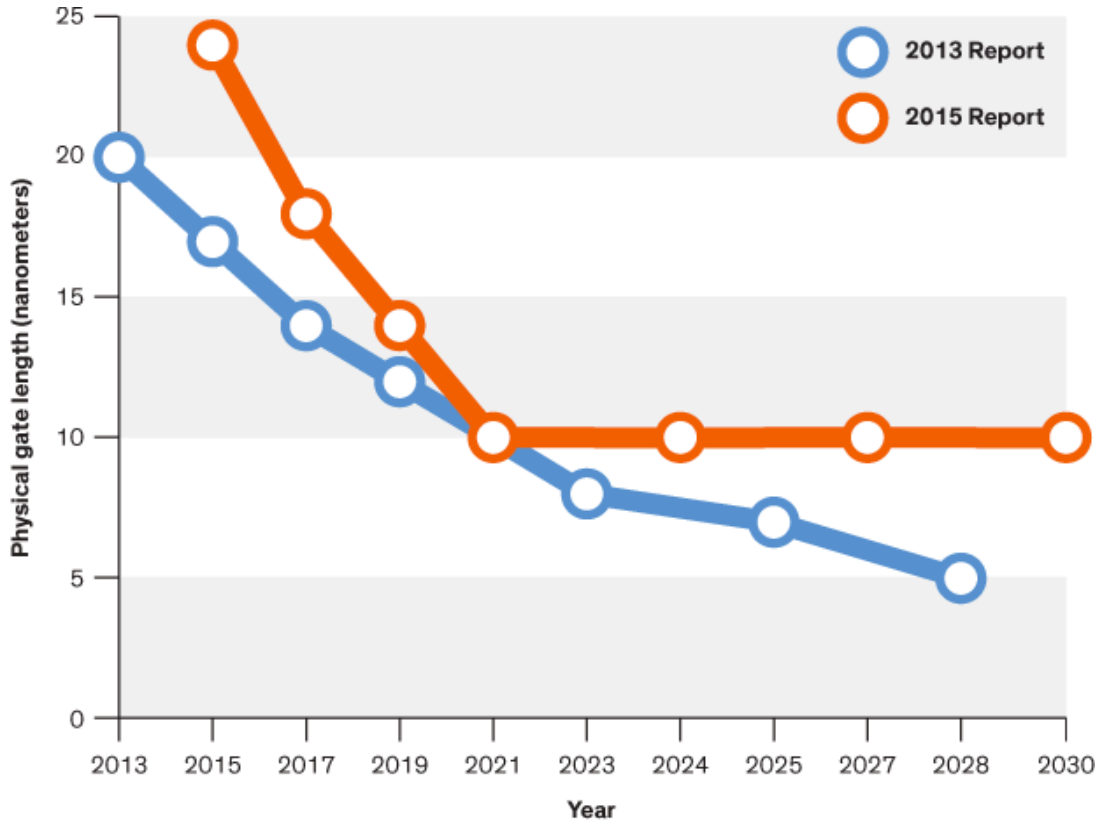
High-k gate dielectric

Tri-Gate transistors with multiple fins connected together increases total drive strength for higher performance

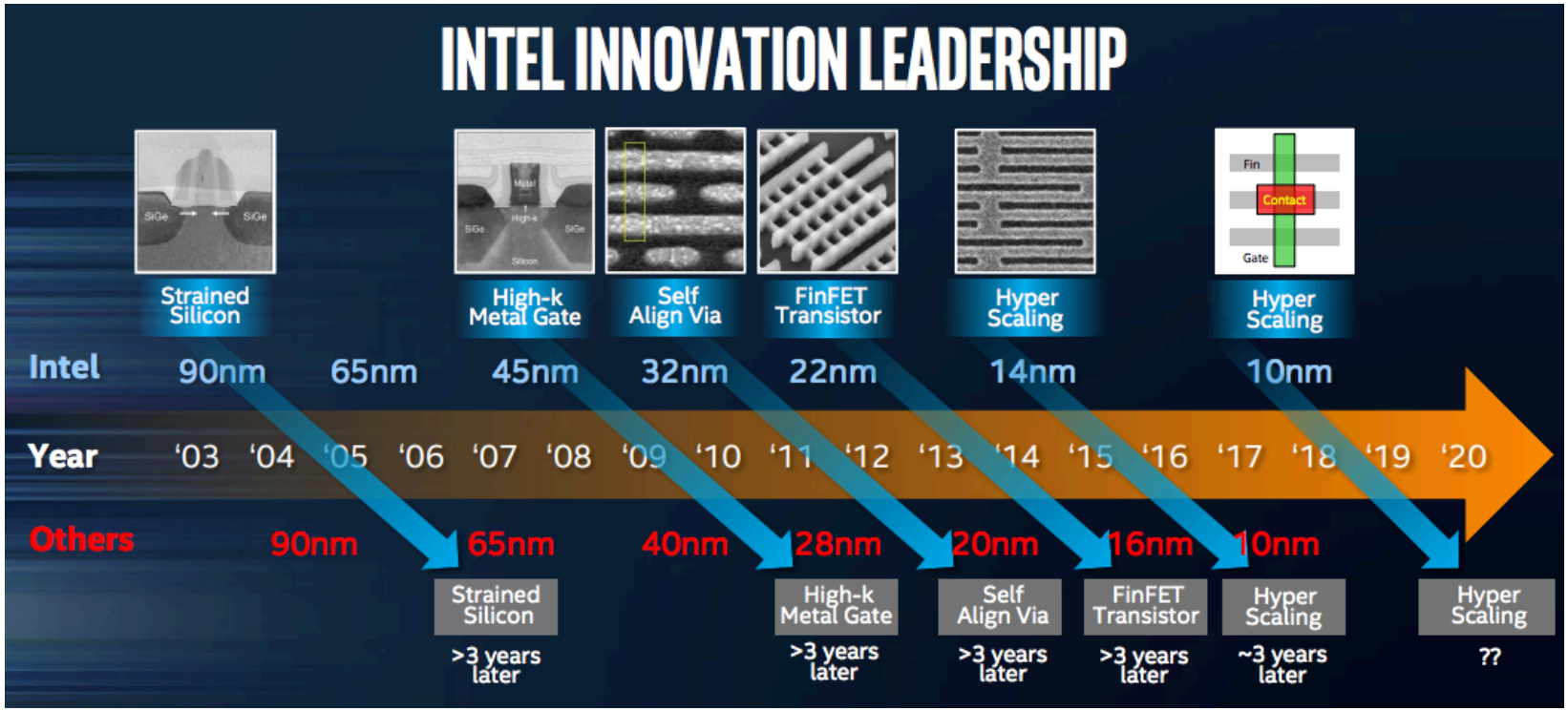
http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf

ITRS 2.0 Report 2015

- "After 2021, the report forecasts, it will no longer be economically desirable for companies to continue traditional transistor miniaturization in microprocessors."

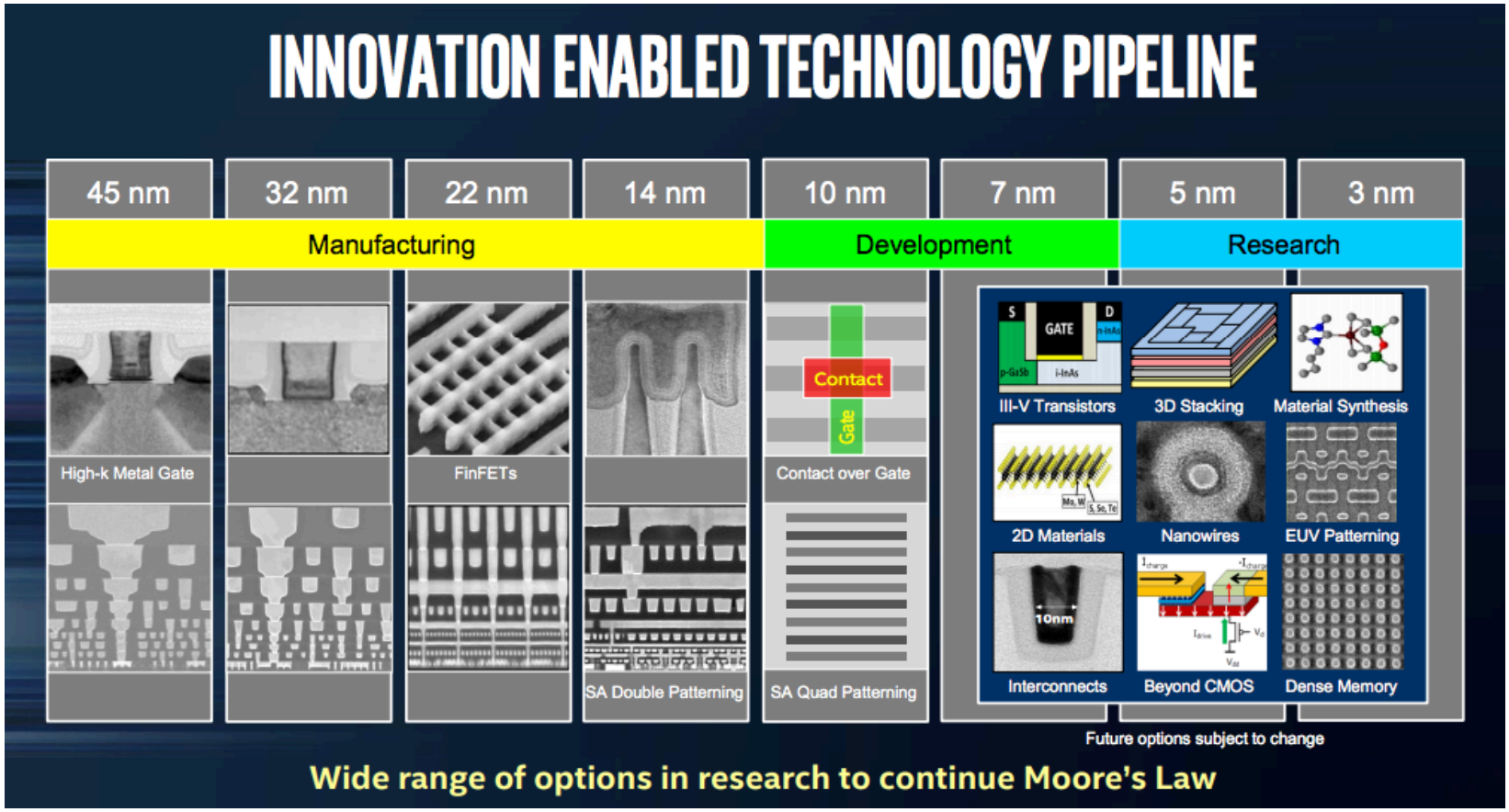


BUT…



Source:https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2020/09/mark-bohr-on-continuing-moores-law.pdf

BUT…

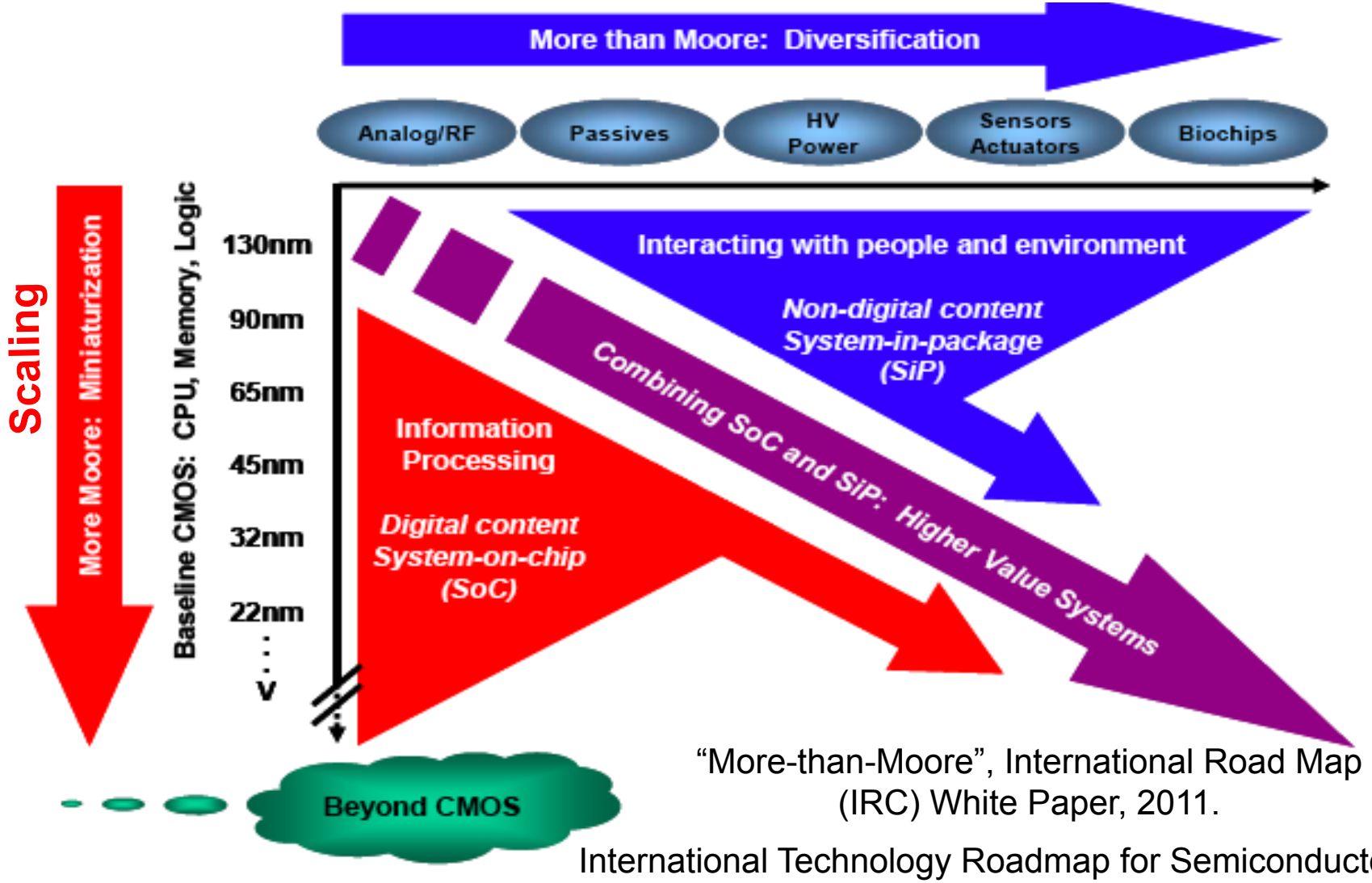


Source:https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2020/09/mark-bohr-on-continuing-moores-law.pdf

More than Moore → Functional Diversification

- Interacting with the outside world
  - Electromagnetic/Optical
    - Radio-frequency domain up to the THz range
    - Optical domain from the infrared to the near ultraviolet
    - Hard radiation (EUV, X-ray, γ-ray)
  - Mechanical parameters (sensors/actuators)
    - MEMS/NEMS position, speed, acceleration, rotation, pressure, stress, etc.
  - Chemical composition (sensors/actuators)
  - Biological parameters (sensors/actuators)
- Power/Energy
  - Integration of renewable sources, Energy storage, Smart metering, Efficient consumption

More-than-Moore

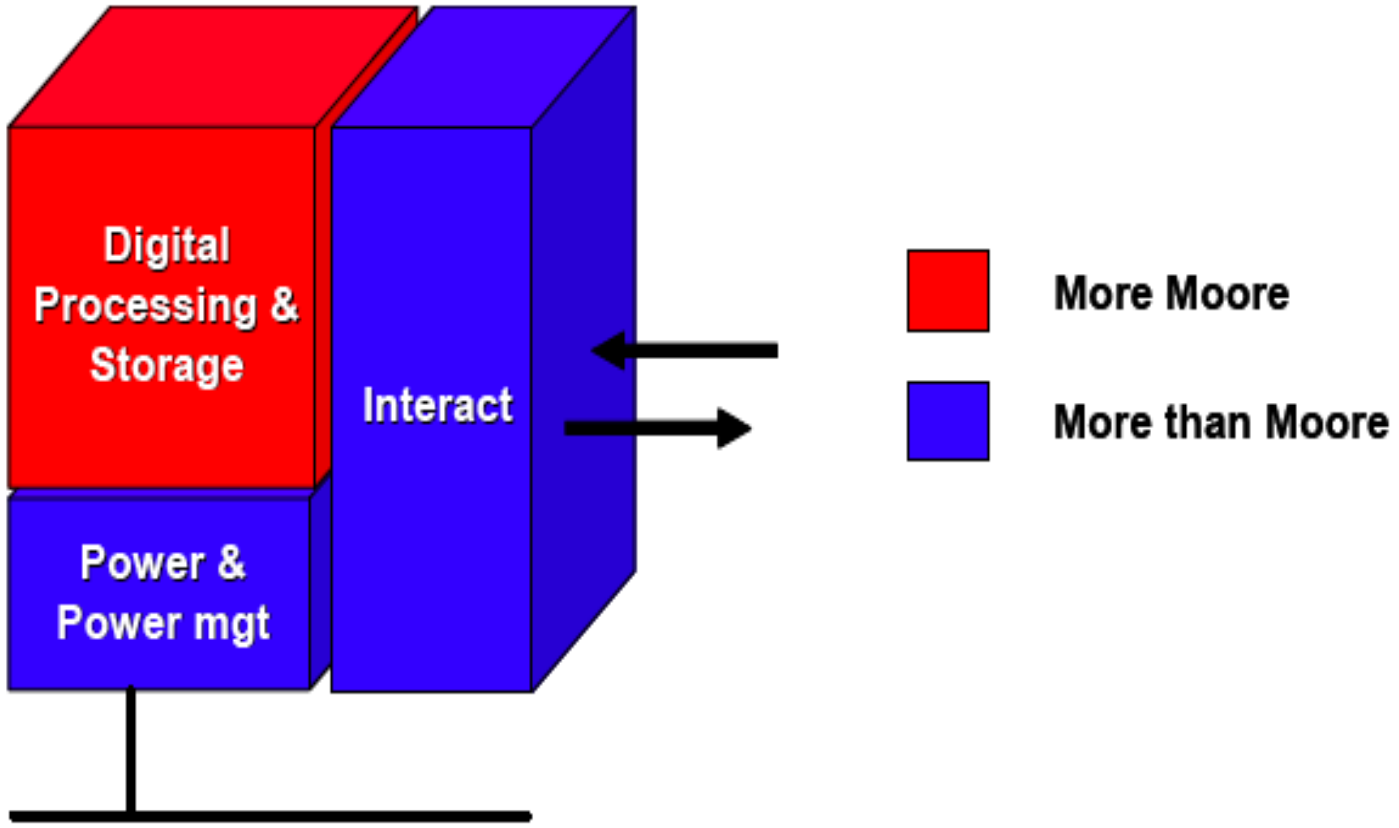


"More-than-Moore", International Road Map (IRC) White Paper, 2011.

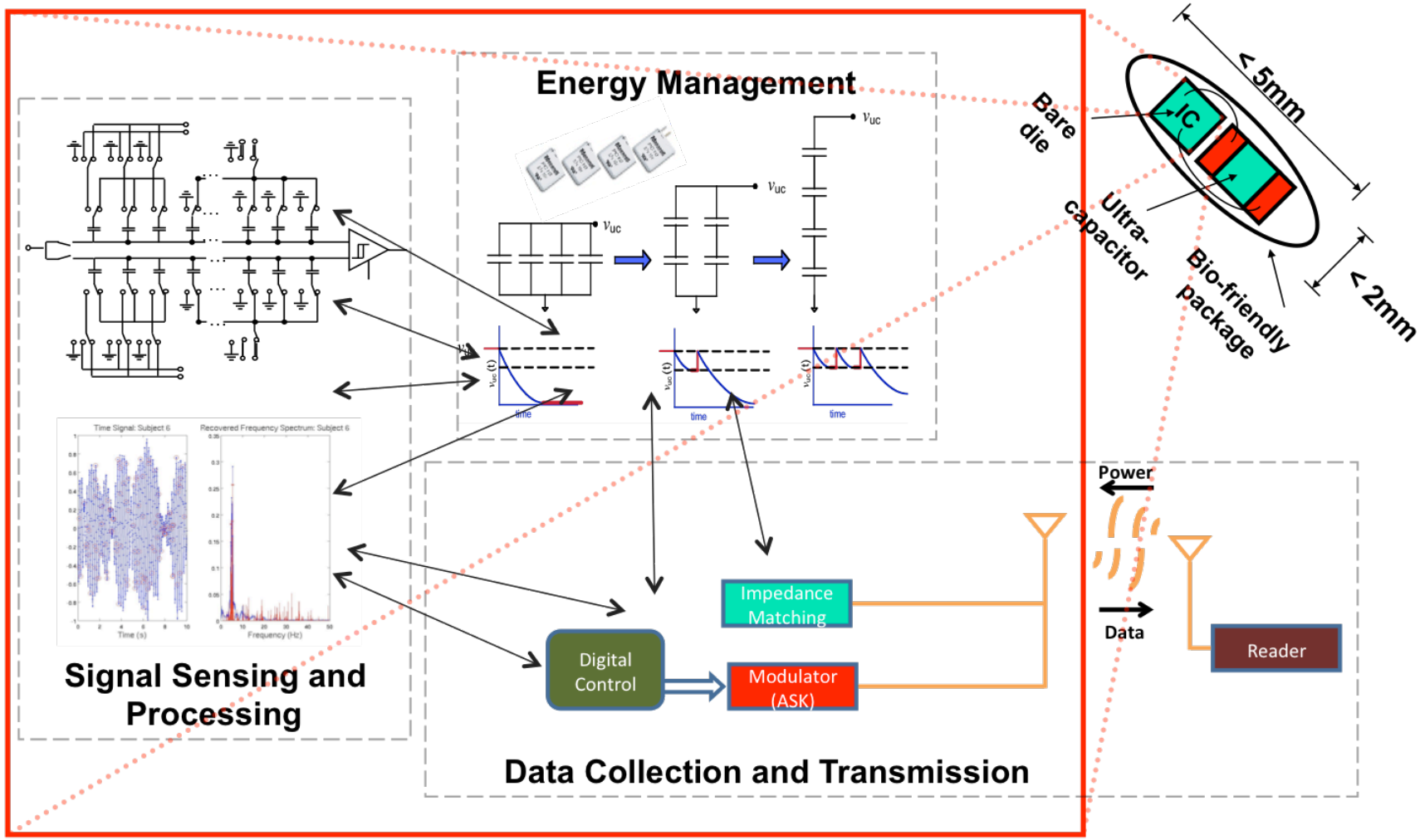
International Technology Roadmap for Semiconductors

"More-than-Moore"

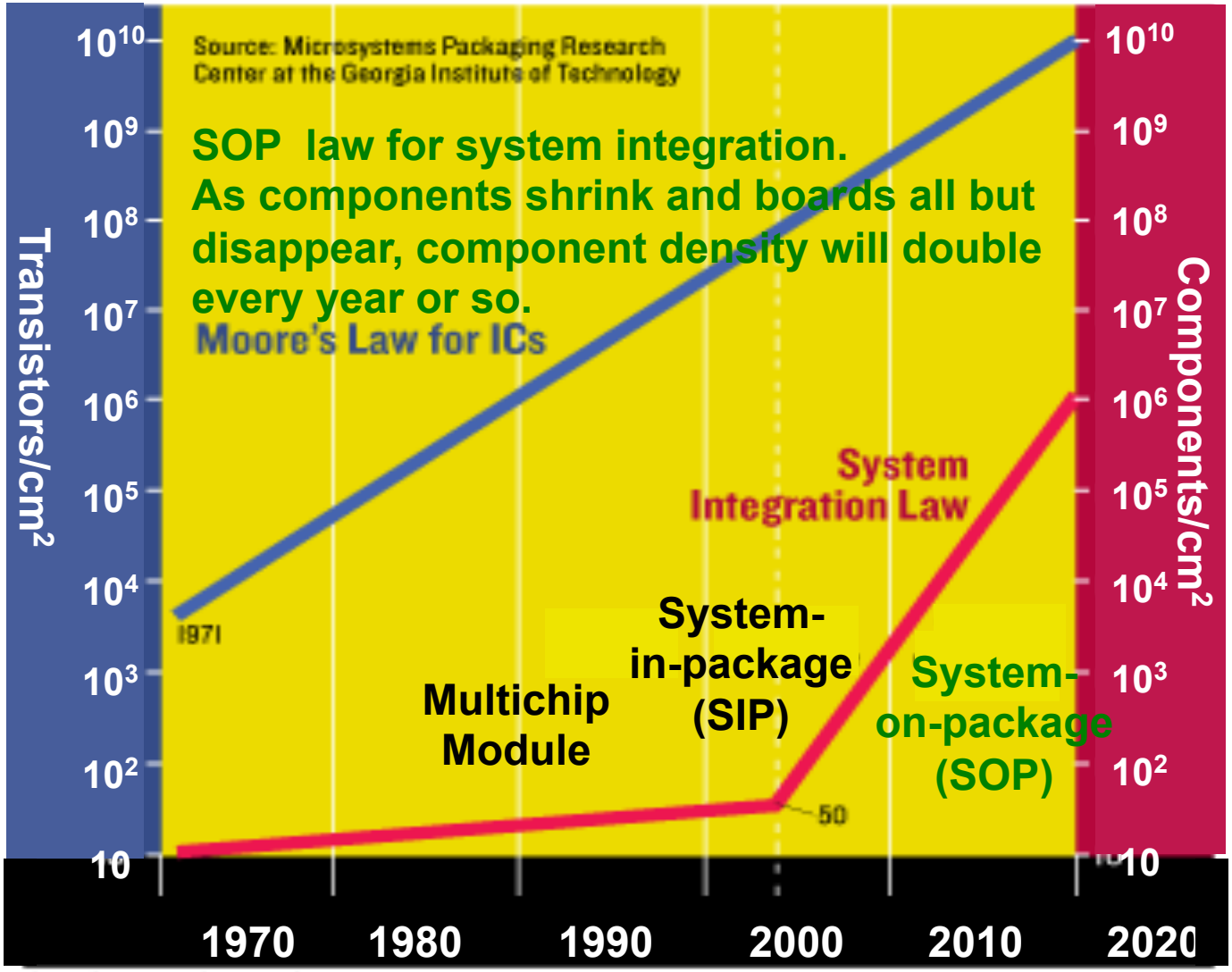
- Components Complement Digital Processing/ Storage Elements in an Integrated System



MicroImplant: An Electronic Platform for Minimally Invasive Sensory Monitors

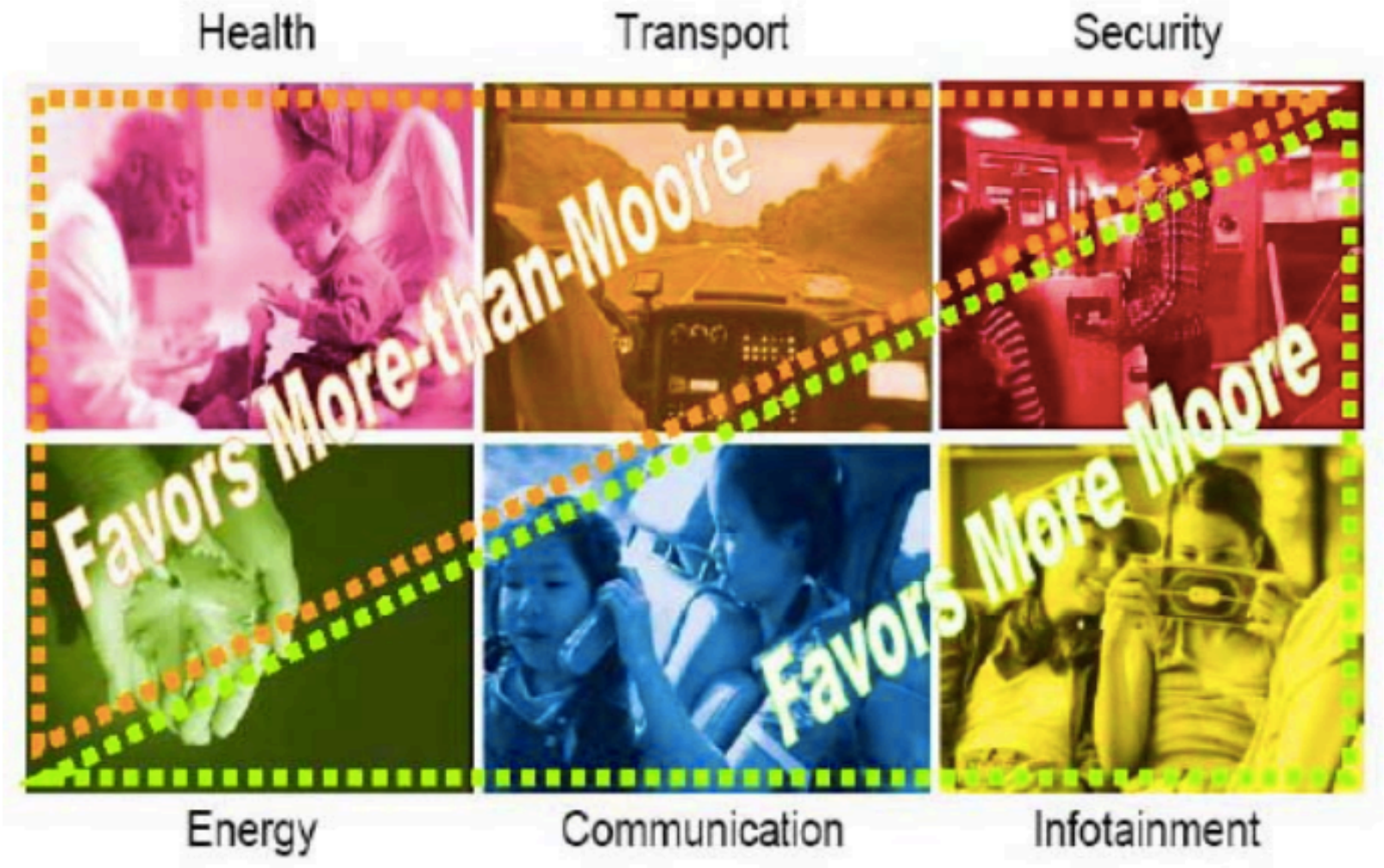


Semiconductor System Integration – More Than Moore's Law



R. Tummala, "Moore's Law Meets Its Match", IEEE Spectrum, June, 2006

Societal Needs

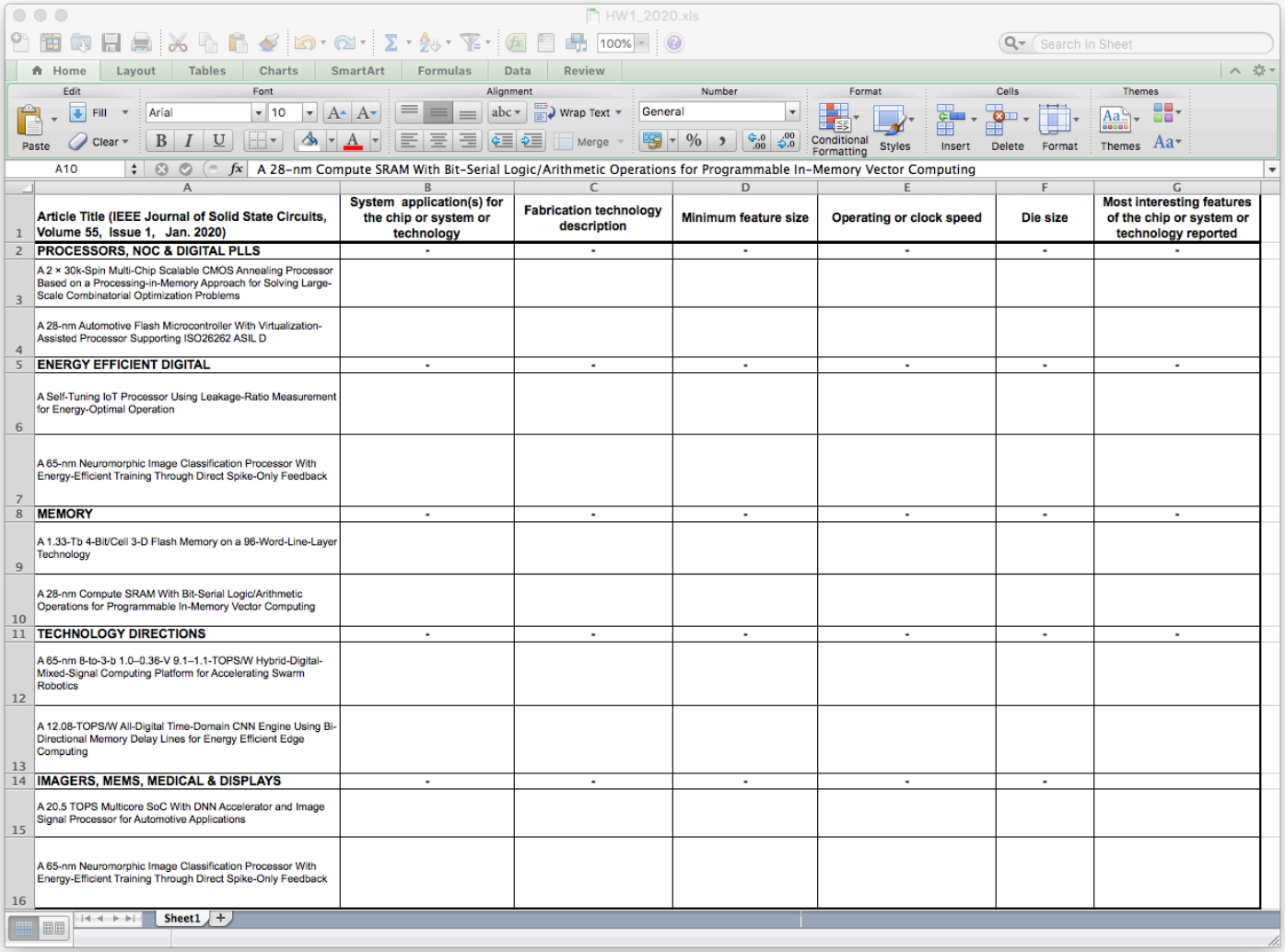


Improvement Trends for VLSI SoCs Enabled by Geometrical and Equivalent Scaling

- TRENDS:
- Higher Integration level
  - exponentially increased number of components/ transistors per chip/package.
- Performance Scaling
  - combination of Geometrical (shrinking of dimensions) and Equivalent (innovation) Scaling.
- System implementation
  - SoC + increased use of SiP -> SOP

- CONSEQUENCES:
- Higher Speed
  - CPU clock rate at multiple GHz + parallel processing.
- Increased Compactness & less weight
  - increasing system integration.
- Lower Power
  - Decreasing energy requirement per function.
- Lower Cost
  - Decreasing cost per function.

Trends in Practice at ISSCC (HW 1)

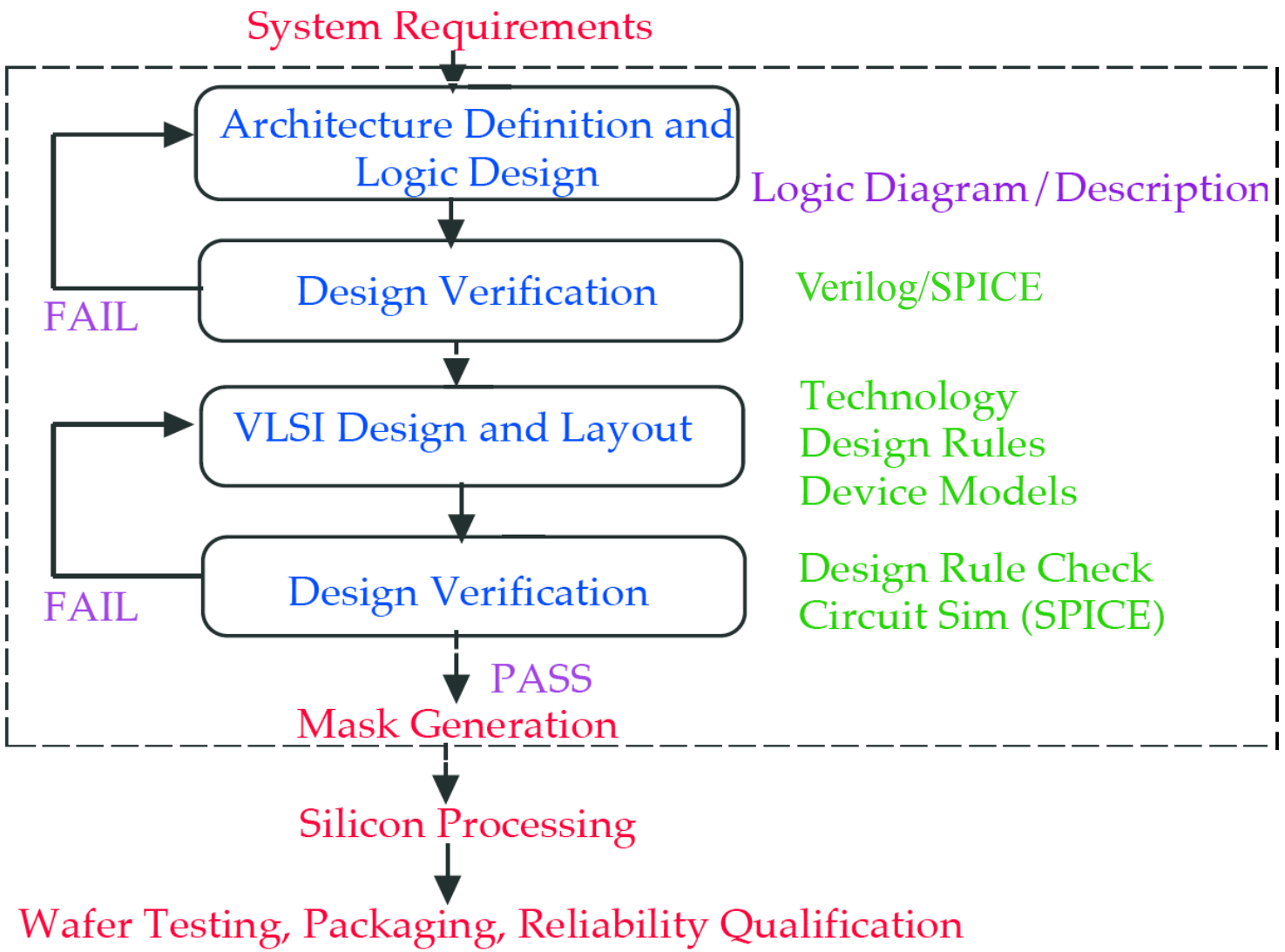


HW1_2020.xls

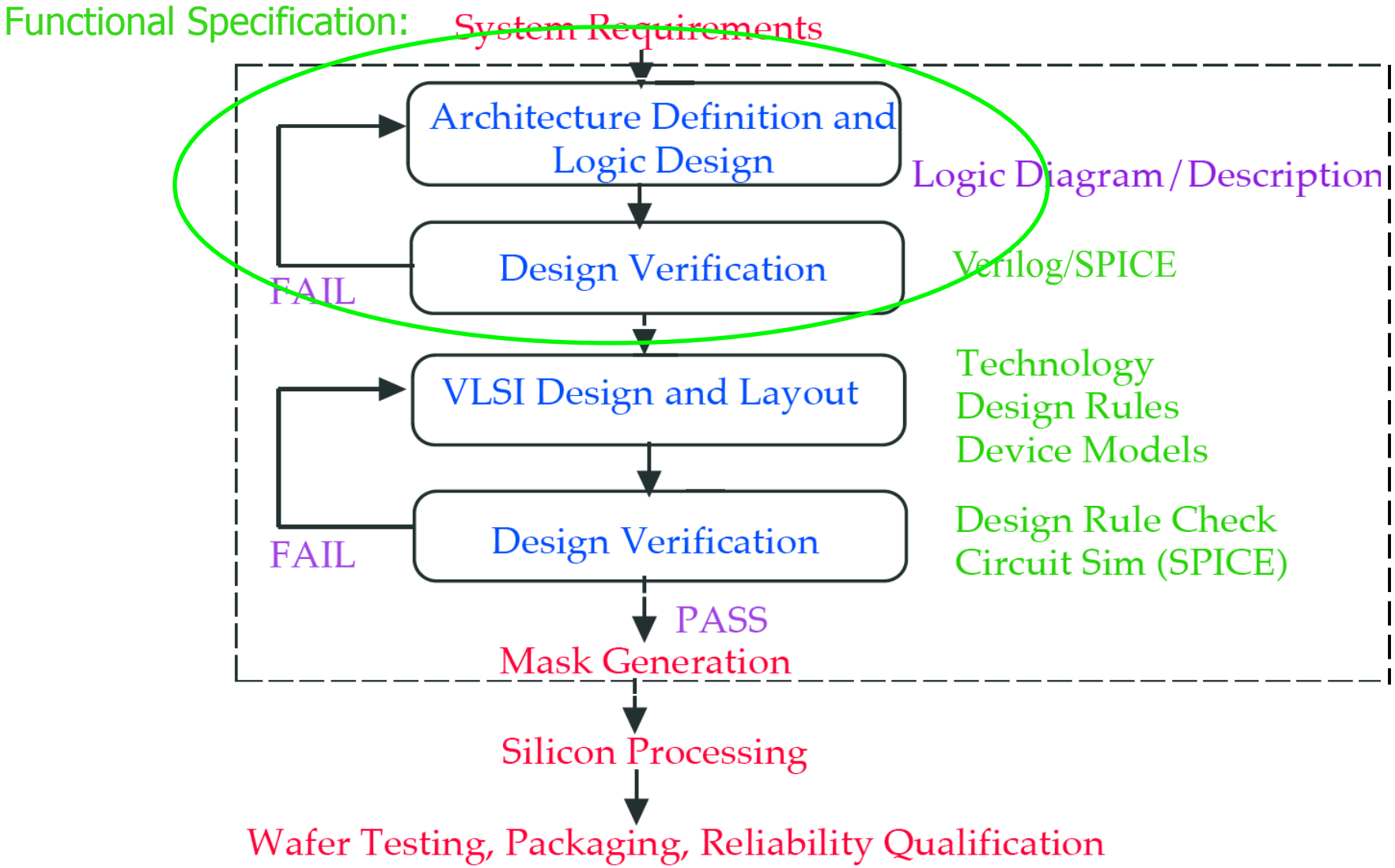
	A	B	C	D	E	F	G
1	**Article Title (IEEE Journal of Solid State Circuits, Volume 55, Issue 1, Jan. 2020)**	**System application(s) for the chip or system or technology**	**Fabrication technology description**	**Minimum feature size**	**Operating or clock speed**	**Die size**	**Most interesting features of the chip or system or technology reported**
2	**PROCESSORS, NOC & DIGITAL PLLS**	-	-	-	-	-	-
3	A 2 × 30k-Spin Multi-Chip Scalable CMOS Annealing Processor Based on a Processing-in-Memory Approach for Solving Large-Scale Combinatorial Optimization Problems						
4	A 28-nm Automotive Flash Microcontroller With Virtualization-Assisted Processor Supporting ISO26262 ASIL D						
5	**ENERGY EFFICIENT DIGITAL**	-	-	-	-	-	-
6	A Self-Tuning IoT Processor Using Leakage-Ratio Measurement for Energy-Optimal Operation						
7	A 65-nm Neuromorphic Image Classification Processor With Energy-Efficient Training Through Direct Spike-Only Feedback						
8	**MEMORY**	-	-	-	-	-	-
9	A 1.33-Tb 4-Bit/Cell 3-D Flash Memory on a 96-Word-Line-Layer Technology						
10	A 28-nm Compute SRAM With Bit-Serial Logic/Arithmetic Operations for Programmable In-Memory Vector Computing						
11	**TECHNOLOGY DIRECTIONS**	-	-	-	-	-	-
12	A 65-nm 8-to-3-b 1.0–0.36-V 9.1–1.1-TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Swarm Robotics						
13	A 12.08-TOPS/W All-Digital Time-Domain CNN Engine Using Bi-Directional Memory Delay Lines for Energy Efficient Edge Computing						
14	**IMAGERS, MEMS, MEDICAL & DISPLAYS**	-	-	-	-	-	
15	A 20.5 TOPS Multicore SoC With DNN Accelerator and Image Signal Processor for Automotive Applications						
16	A 65-nm Neuromorphic Image Classification Processor With Energy-Efficient Training Through Direct Spike-Only Feedback						

Design Example

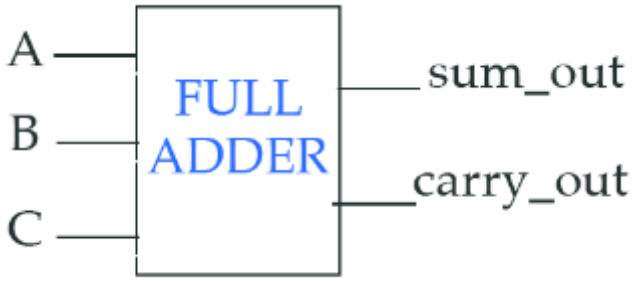
VLSI Design Cycle or Flow



VLSI Design Cycle or Flow



Illustrative Circuit Design Example: System Requirements



Input Variables:

addends: A, B

carry-in: C

Output Variables:

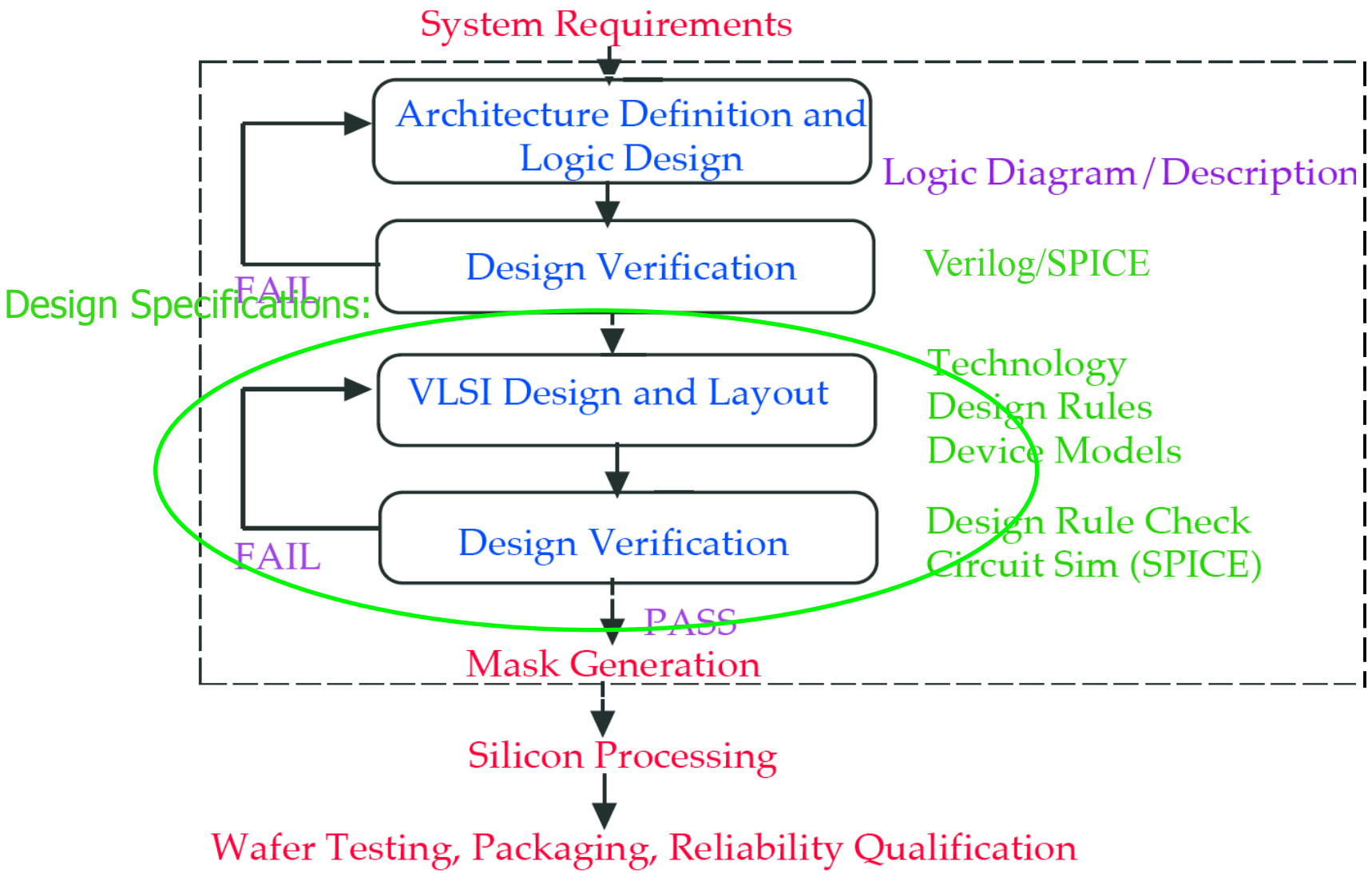
sum_out, carry_out

Functional Specification:

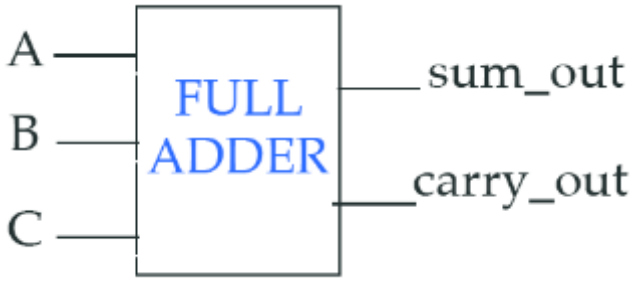
$$\text{sum\_out} = A \oplus B \oplus C = ABC + A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{C}B$$

$$\text{carry\_out} = AB + AC + BC$$

VLSI Design Cycle or Flow



Illustrative Circuit Design Example: System Requirements



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Functional Specification:

$$\text{sum\_out} = A \oplus B \oplus C = ABC + A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{C}B$$

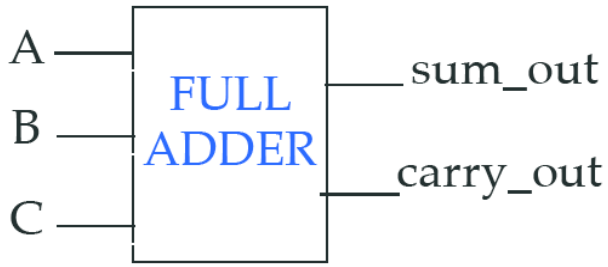
$$\text{carry\_out} = AB + AC + BC$$

Design Specifications (in 0.8 twin-well CMOS):

1. Propagation Delay Times of SUM and CARRY_Out signals: $\leq$ 1.2 ns
2. Rise and Fall Times of SUM and CARRY_Out signals: $\leq$ 1.2 ns
3. Circuit Die Area: $\leq$ 1500 um^2
4. Dynamic Power Dissipation (@ V_{DD} = 5 V and f_{max} = 20 MHz): $\leq$ 1 mW

Illustrative Circuit Design Example: Architecture Definition

START: Boolean description of binary adder circuit:



A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

DEFINE:

Input Variables:

addends: A, B

carry-in: C

Output Variables:

sum_out, carry_out

BOOLEAN FUNCTION:

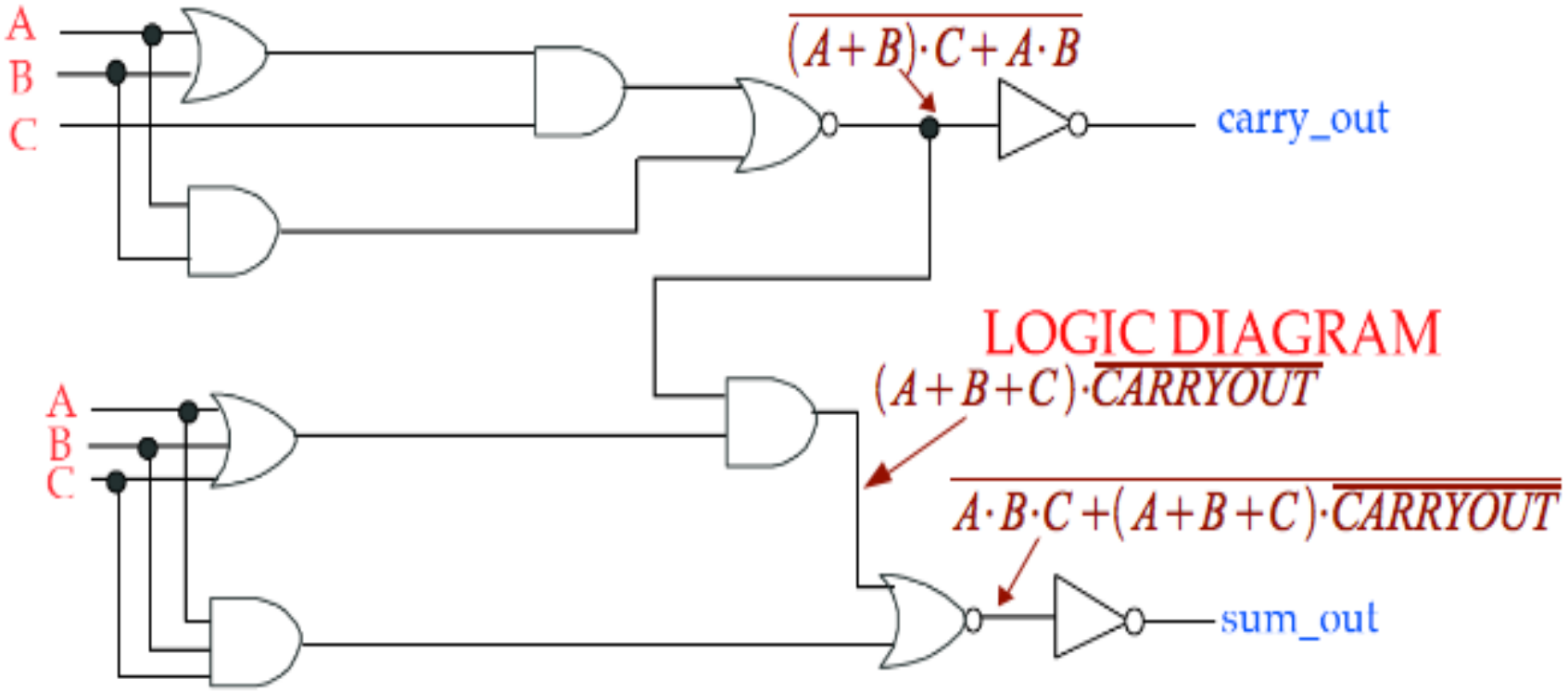
$$\text{sum\_out} = A \oplus B \oplus C = ABC + A\overline{BC} + \overline{AB}C + \overline{AC}B = ABC + (A + B + C)\,\overline{\text{carry\_out}}$$

$$\text{carry\_out} + AB + AC + BC$$

Use of carry_out to realize sum_out reduces circuit complexity and die area.

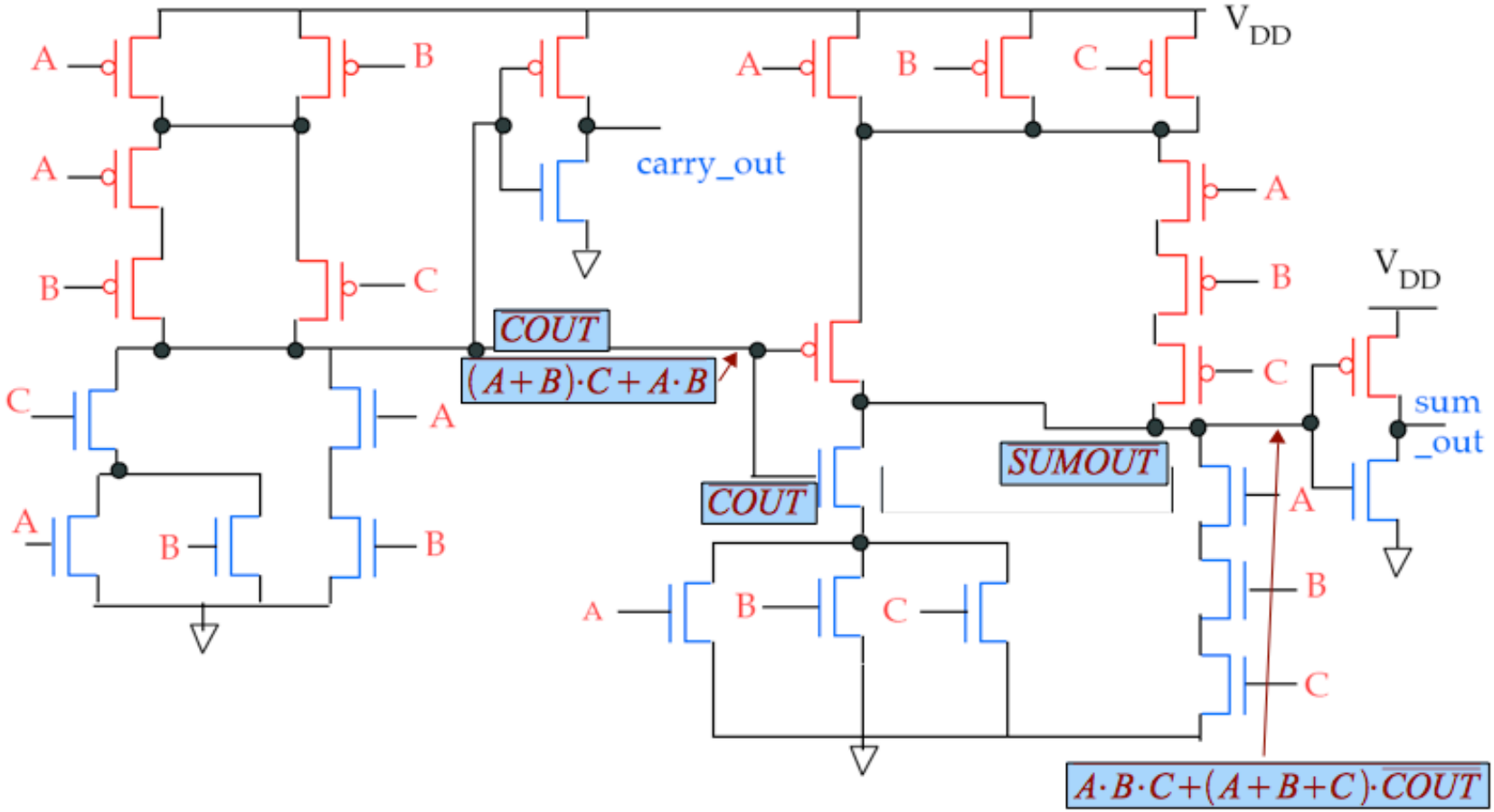
Illustrative Circuit Design Example: Logic Design

- Gate Level Schematic of One-Bit Full Adder Circuit



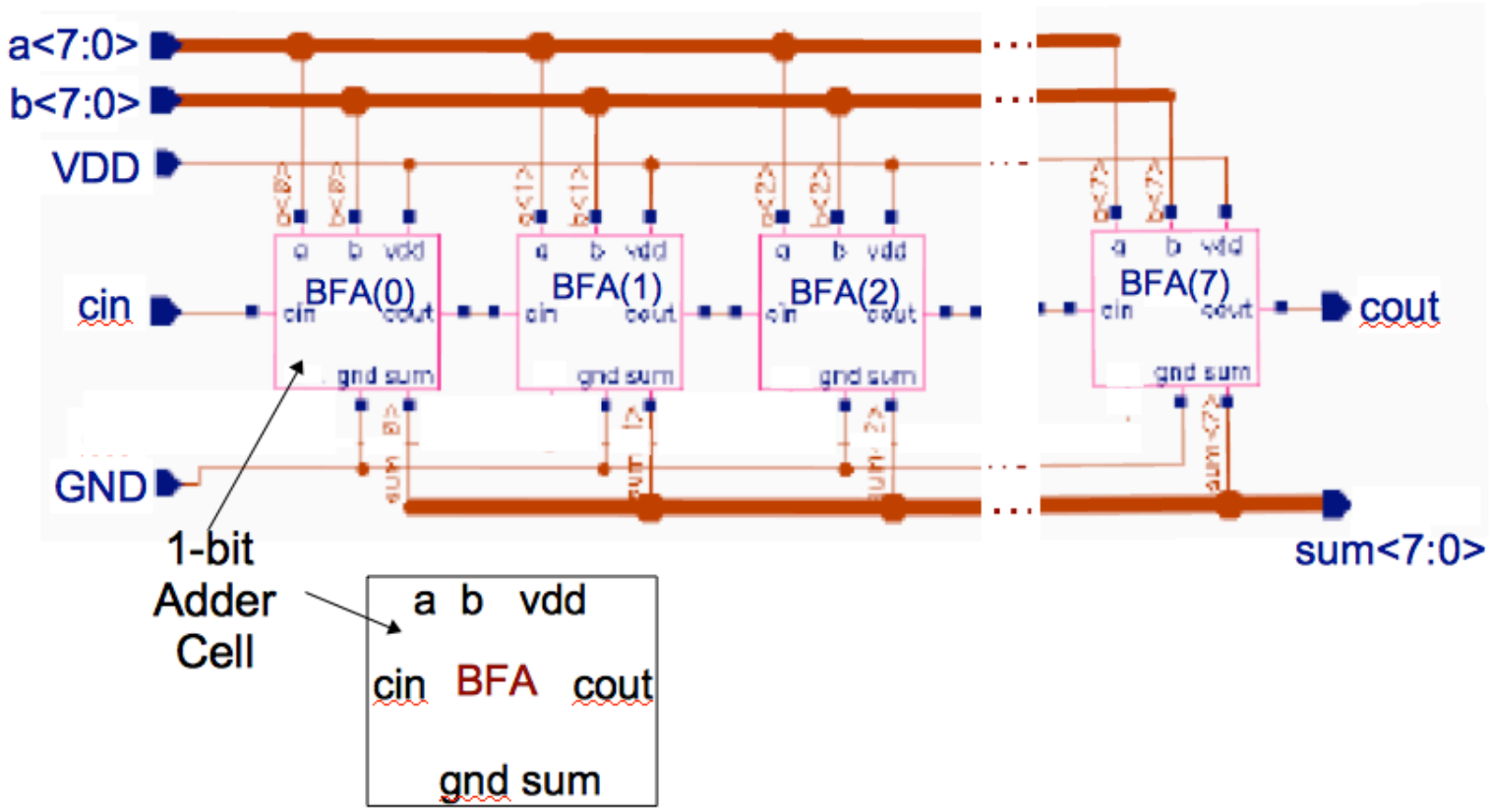
Illustrative Circuit Design Example: VLSI Design

- Transistor Level Schematic of One-Bit Full Adder Circuit

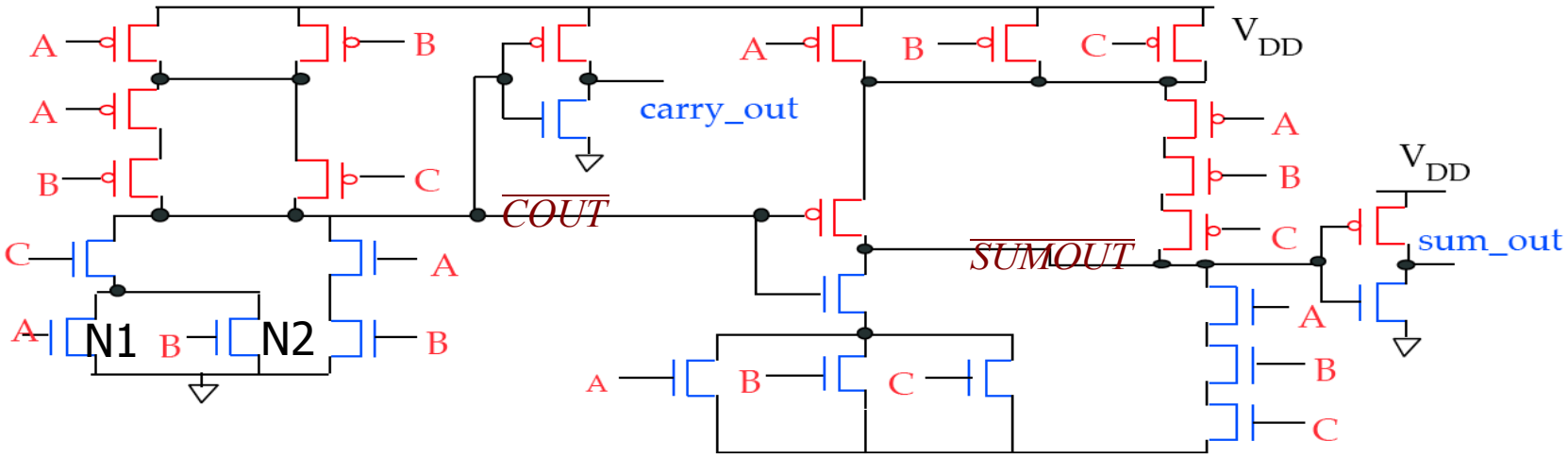


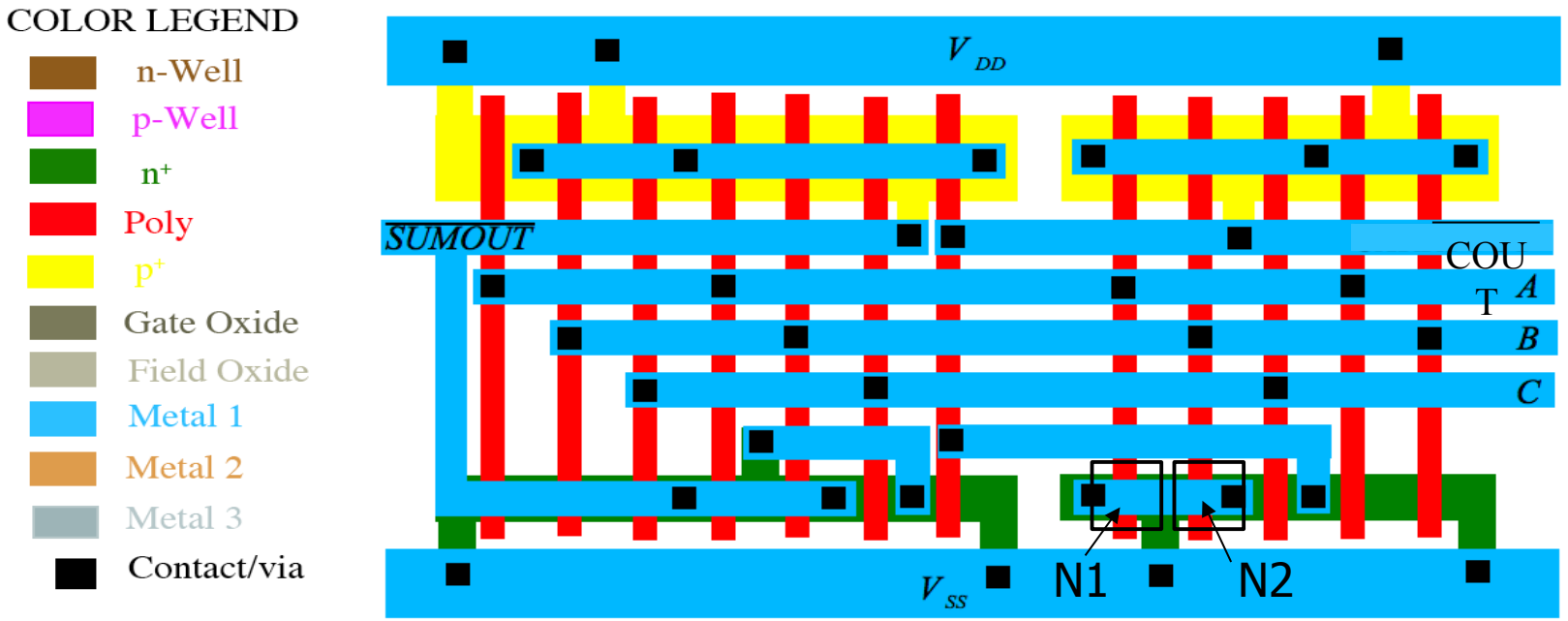
Illustrative Circuit Design Example: VLSI Design

- 8-bit Ripple Adder



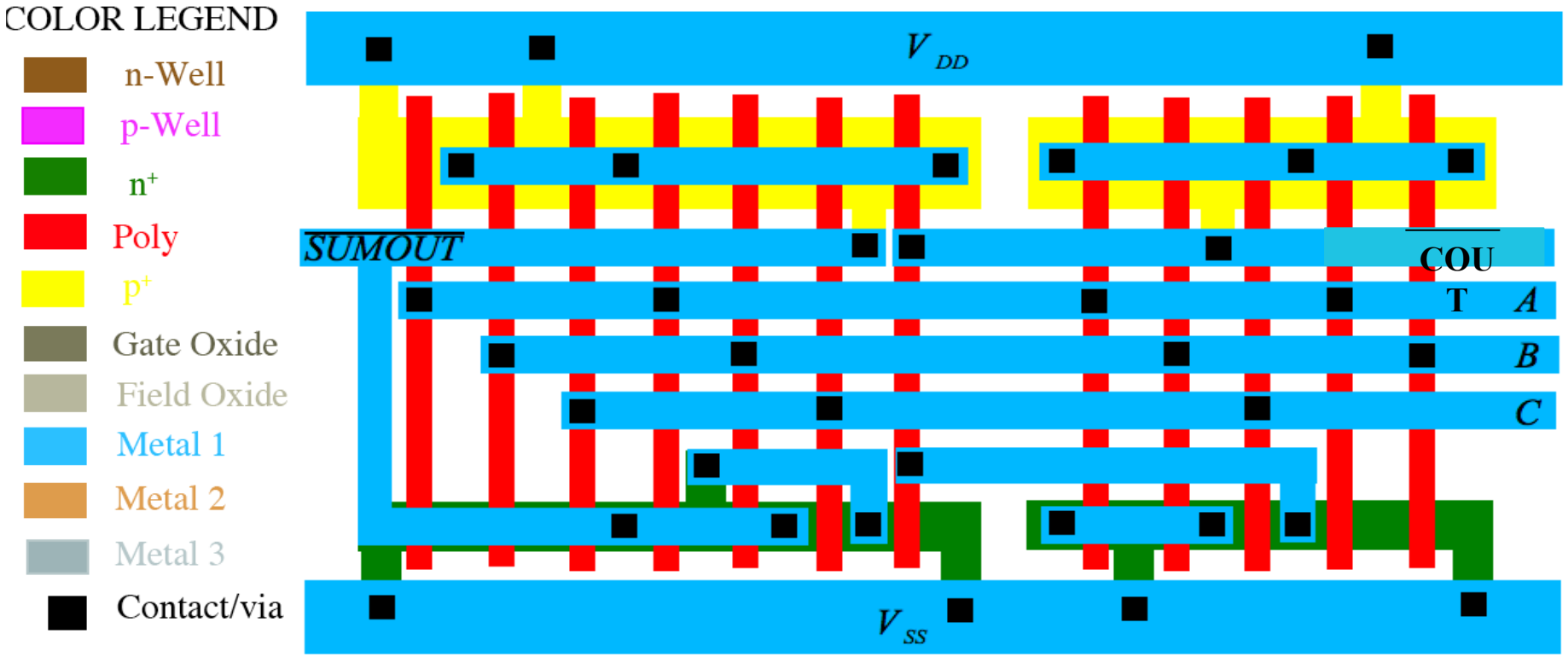
Illustrative Circuit Design Example: VLSI Design and Layout





Illustrative Circuit Design Example: VLSI Design and Layout

- Initial Layout of One-Bit Full Adder Circuit

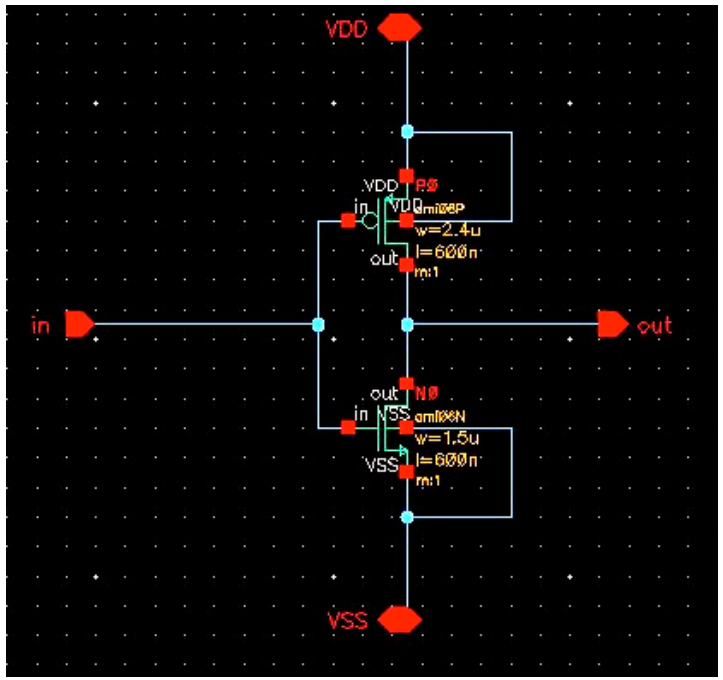


Layout with W/L = 2 µm/0.8 µm

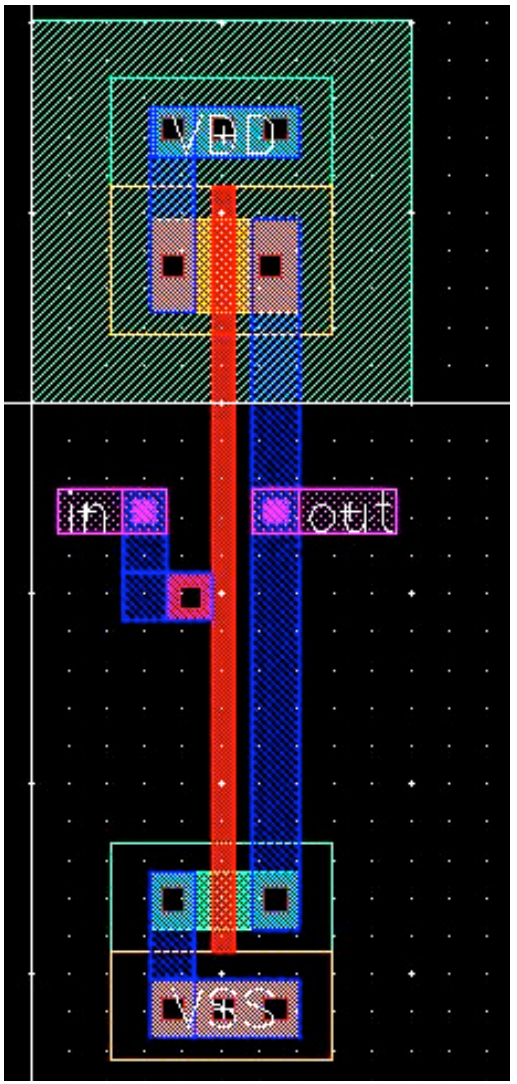
Area 21 µm x 54 µm = 1134 µm^2 ≤ 1500 um^2

Dynamic Power Dissipation (@ V_{DD} = 5V, f_{max} = 20 MHz): = 0.7 mW ≤ 1 mW

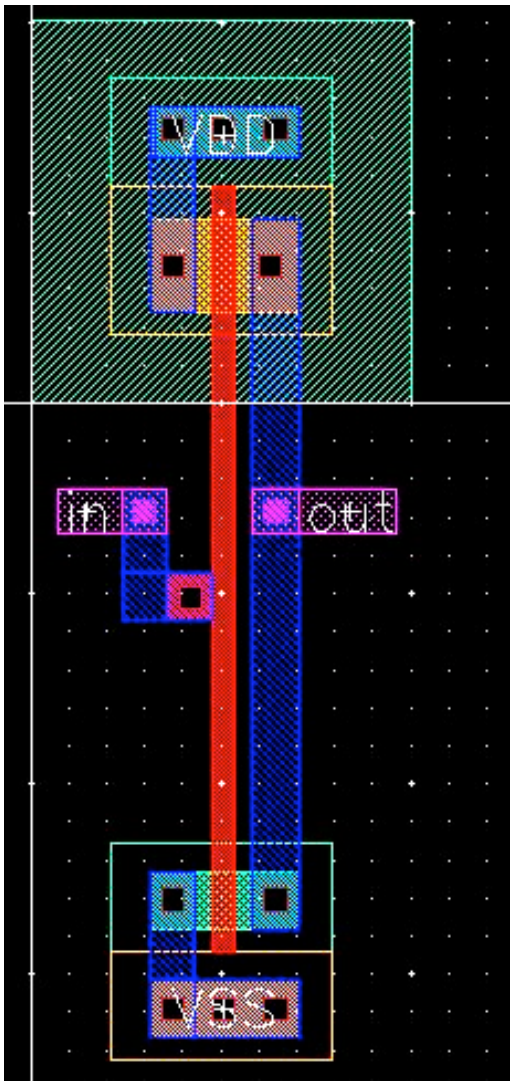
Post Layout Simulation (Analog extracted)



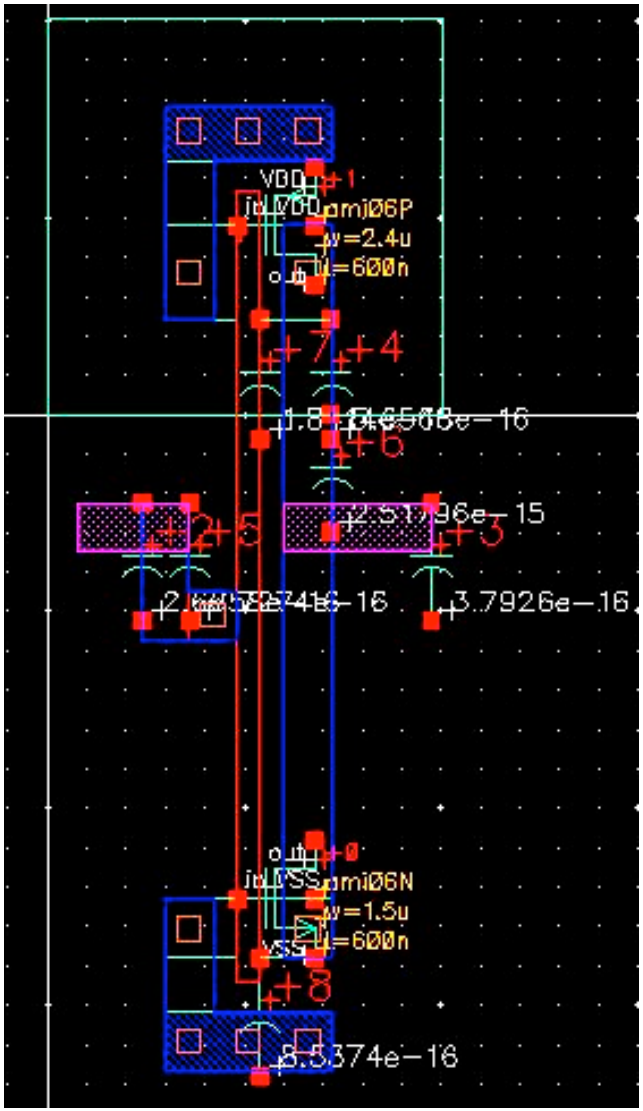
Schematic to layout



Post Layout Simulation (Analog extracted)



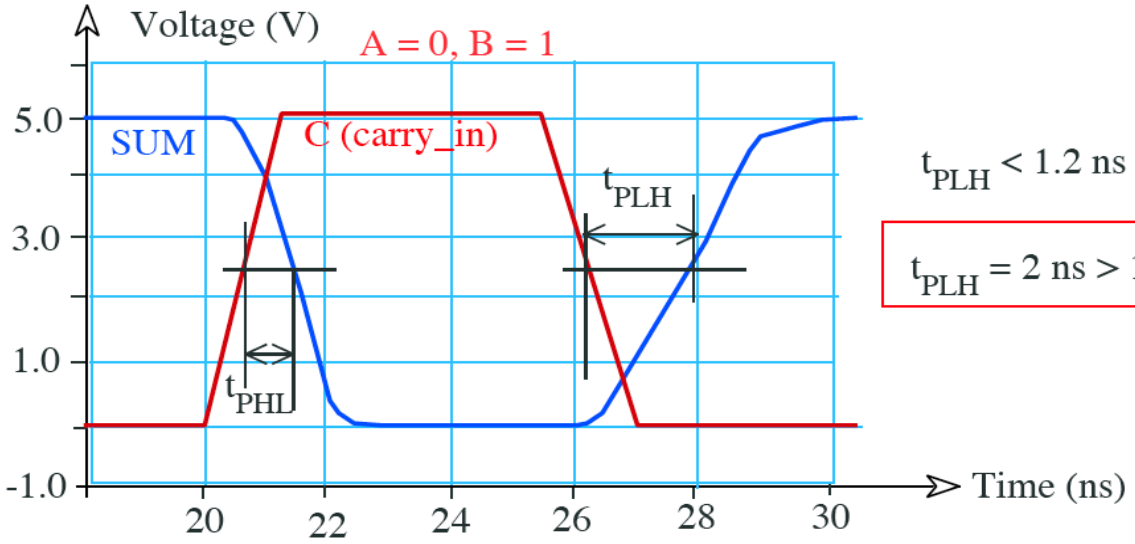
Layout to schematic



Illustrative Circuit Design Example: Design Verification

SPECIFICATIONS:
1. Propogation Delay Times of SUM & CARRY_OUT signals: ≤ 1.2 ns
2. Transition Delay Times of SUM & CARRY_OUT signals: ≤ 1.2 ns
3. Circuit Die Area: ≤ 1500 µm²
4. Dynamic Power Dissipation (@ V_{DD} = 5 V and f_{max} = 20 MHz): ≤ 1 mW

Layout with W/L = 2 µm/0.8 µm



t_{PLH} < 1.2 ns

t_{PLH} = 2 ns > 1.2 ns

Spec NOT met

Modified Layout Required

1. Increase W/L's of transistors
2. Consider more compact placement of transistors and reduce interconnect in critcal paths

Admin

- Find web, get text, assigned reading…
  - http://www.seas.upenn.edu/~ese570
  - https://piazza.com/upenn/spring2020/ese570/
  - https://canvas.upenn.edu/
- HW 1 posted now
  - Due next week 1/24
- Remaining Questions?