

Rent's Rule Based Switching Requirements

Prof. André DeHon
<andre@cs.caltech.edu>
California Institute of Technology



DeHon March 2001

Questions

Conventional GA/ASIC/VLSI:

- How much wiring do I need to support my logic?
 - How does this scale with larger designs?

For reconfigurable devices (FPGA, PSoC)

- (also) How much switching do I need to support my logic?
 - How does this scale with larger designs?

DeHon March 2001

Answers

- First question (wiring):
 - answer with Rent's Rule characterization
 - subject of prior talks
- Second question (switches)
 - can also approach in terms of Rent's Rule
 - that's what this talk is about

DeHon March 2001

Why?

- With the silicon capacity available today, we find that we
 - can build large, high performance, spatial computing organizations
 - need flexibility in our large system chips
 - build large
 - FPGAs
 - spatially configurable devices
 - Programmable SoC designs
 - single-chip multiprocessors

DeHon March 2001

Why?

Components with spatial flexibility
(FPGAs, PSoCs, multiprocessors)

- need efficient, switchable interconnect

DeHon March 2001

Outline

- Need
- Problem
- Review
 - General case expensive
 - Rent's Rule as a measure of locality
 - Impact on wiring
- Impact on Switching
 - practical issues
 - design space
- Summary

DeHon March 2001

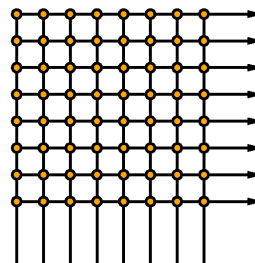
Problem

- **Given:** Graph of operators
 - gates, PEs, memories, ...
 - today: 100 PEs, 100,000 FPGA 4-LUTs
- **Goal:** Implement “any” graph on programmable substrate
 - provide flexibility
 - while maintaining efficiency, compact implementation

DeHon March 2001

Challenge

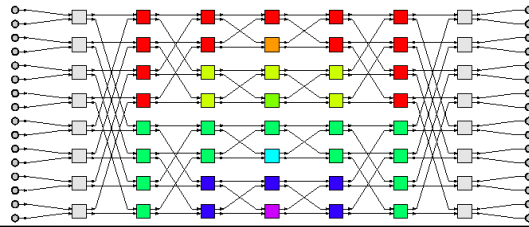
- “Obvious” direct solutions
 - are prohibitively expensive
 - scale poorly
- *E.g.* Crossbar
 - $O(n^2)$ area and delay
 - density and performance decrease as we scale upward



DeHon March 2001

Multistage Networks

- Can reduce switch requirements
 - at cost of additional series switch latency
- E.g. Beneš Network
 - implement any permutation
 - $O(N \log(N))$ switches, $O(\log(N))$ delay



DeHon March 2001

Multistage Wiring

- Wiring area in 2D-VLSI still $O(n^2)$
 - bisection width of Beneš (all flat MINs) is $O(n)$
 - $O(n)$ wires cross middle of chip
 - with constant layers
 - will imply $O(n)$ chip width
 - true when consider next dimension
 - chip is $O(n) \times O(n)$ or $O(n^2)$ wiring area

DeHon March 2001

With “Flat” Networks

- Density diminishes as designs increase
 - $O(N \log(N))$ switches for N nodes
 - $O(N^2)$ wiring for N nodes

DeHon March 2001

Locality Structure

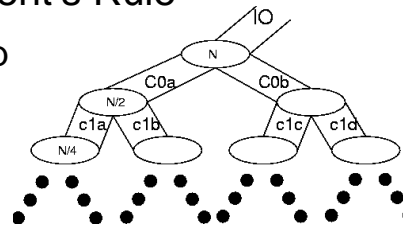
- Is this the problem we really need to solve?
- Or, is there additional structure in our (typical) designs?
 - allows us to get away with less?

DeHon March 2001

Rent's Rule

- Characterization of Rent's Rule

$$IO = c N^p$$

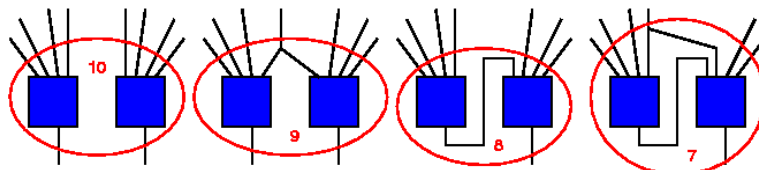


- Says:
 - typical graphs are not random
 - when we have freedom of placement
 - can contain some connections in a local region

DeHon March 2001

Rent's Rule and Locality

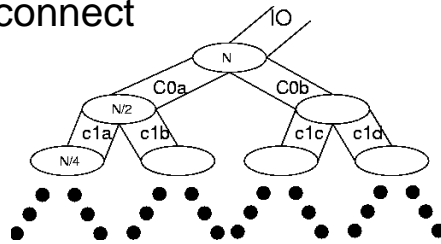
- Rent and IO capture locality
 - local consumption
 - local fanout



DeHon March 2001

Locality Measure

- View of Rent's Rule:
 - quantifies the locality in a design
 - smaller p
 - more locality
 - less interconnect



DeHon March 2001

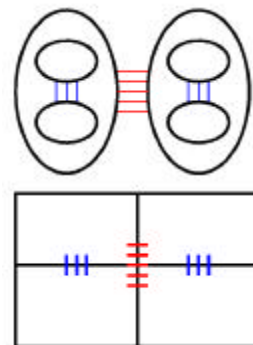
Traditional Use

- Use Rent's Rule characterization to understand wire growth

$$IO = c N^p$$

- Top bisections will be $\Omega(N^p)$
- 2D wiring area

$$\Omega(N^p) \times \Omega(N^p) = \Omega(N^{2p})$$



DeHon March 2001

We Know

- How we avoid $O(N^2)$ wire growth for “typical” designs
- How to characterize locality
- How we exploit that locality to reduce wire growth
- Wire growth implied by a characterized design

DeHon March 2001

Switching:

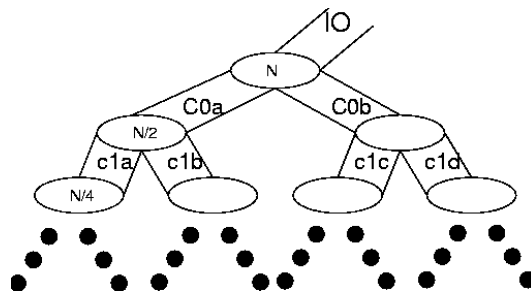
How can we use the locality captured by Rent's Rule to reduce switching requirements? (How much?)

DeHon March 2001

Observation

- Locality that saved us wiring,
also saves us switching

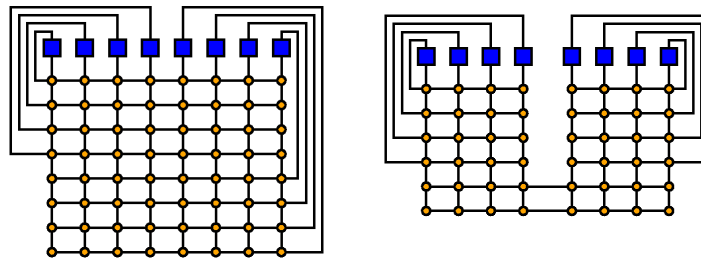
$$IO = c N^p$$



DeHon March 2001

Consider

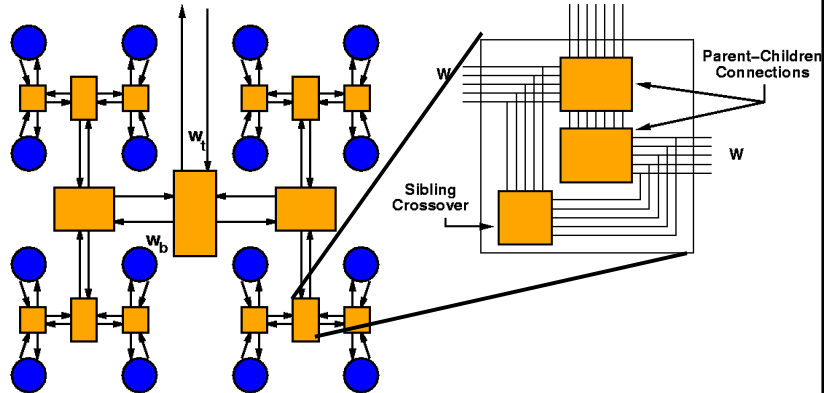
- Crossbar case to exploit wiring:
 - split into two halves
 - $N/2 \times N/2$ crossbar each half
 - $N/2 \times (N/2)^p$ connect to bisection wires



DeHon March 2001

Recurse

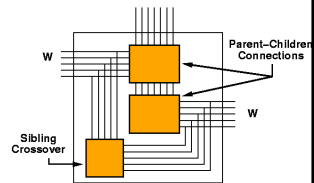
- Repeat at each level
 - form tree



DeHon March 2001

Result

- If use crossbar at each tree node
 - $O(N^{2p})$ wiring area
 - $p > 0.5$, direct from bisection
 - $O(N^{2p})$ switches
 - top switch box is $O(N^{2p})$
 - switches at one level down is
 - $2 \times (1/2^p)^2$ x previous level
 - coefficient < 1 for $p > 0.5$
 - get geometric series; sums to $O(1)$



DeHon March 2001

Good News

- Good news
 - asymptotically optimal
 - Even without switches area $O(N^{2p})$
 - so adding $O(N^{2p})$ switches not change

DeHon March 2001

Bad News

- Switches area \gg wire crossing area
 - Consider 6λ wire pitch \Rightarrow crossing $36 \lambda^2$
 - Typical (passive) switch $\Rightarrow 2500 \lambda^2$
 - Passive only: 70x area difference
 - worse once rebuffer or latch signals.
- Switches limited to substrate
 - whereas can use additional metal layers for wiring area

DeHon March 2001

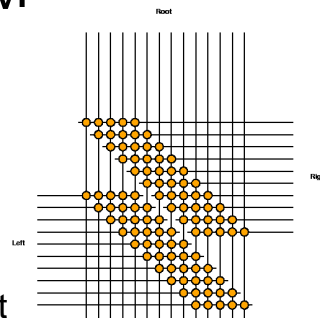
Additional Structure

- This motivates us to look beyond crossbars
 - can depopulate crossbars on up-down connection without loss of functionality
 - can replace crossbars with multistage networks

DeHon March 2001

N-choose-M

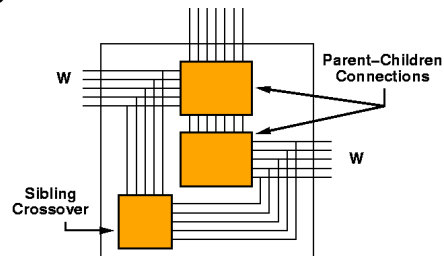
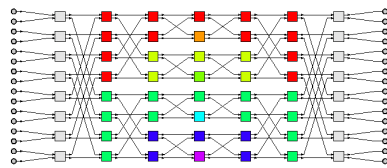
- Up-down connections
 - only require concentration
 - choose M things out of N
 - not full option for placement
 - *i.e.* order of subset irrelevant
- Consequent:
 - can save a constant factor $\sim 2^p/(2^p-1)$
 - $(N/2)^p \times N^p$ vs $(N^p - (N/2)^{p+1})(N/2)^p$
- Similar, Left-Right
 - order not important \Rightarrow reduces switches



DeHon March 2001

Beneš Switching

- Flat networks reduced switches
 - N^2 to $N(\log(N))$
 - using multistage network
- Replace crossbars in tree with Beneš switching networks



DeHon March 2001

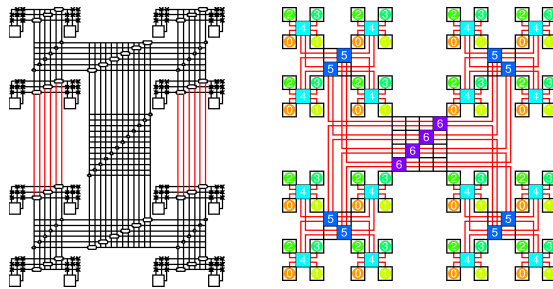
Beneš Switching

- Implication of Beneš Switching
 - still require $O(W^2)$ wiring per tree node
 - or a total of $O(N^{2p})$ wiring
 - now $O(W \log(W))$ switches per tree node
 - converges to $O(N)$ total switches!
 - $O(\log^2(N))$ switches in path across network
 - strictly speaking, dominated by wire delay $\sim O(N^p)$
 - but constants make of little practical interest except for very large networks

DeHon March 2001

Linear Switch Population

- Can further reduce switches
 - connect each lower channel to $O(1)$ channels in each tree node
 - end up with $O(W)$ switches per tree node



DeHon March 2001

Linear Consequences: Good News

- Linear Switches
 - $O(\log(N))$ switches in path
 - $O(N^{2p})$ wire area
 - $O(N)$ switches
 - More practical than Beneš case

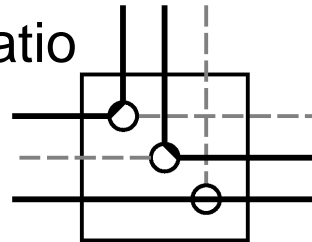
DeHon March 2001

Linear Consequences: Bad News

- Lacks guarantee can use all wires
 - as shown, at least mapping ratio > 1
 - likely cases where even **constant** not suffice
 - expect no worse than logarithmic
 - open to establish tight lower bound for **any** linear arrangement
- Finding Routes is harder
 - no longer linear time, deterministic
 - open as to exactly how hard

DeHon March 2001

Mapping Ratio

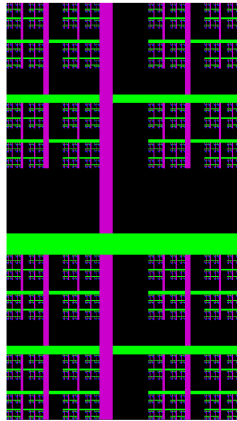


- Mapping ratio says
 - if I have W channels
 - may only be able to use W/mr wires
 - for a particular design's connection pattern
 - to accommodate any design
 - for all channels
- physical wires $\geq mr \times$ logical

DeHon March 2001

Area Comparison

Both:
 $p=0.67$
 $N=1024$



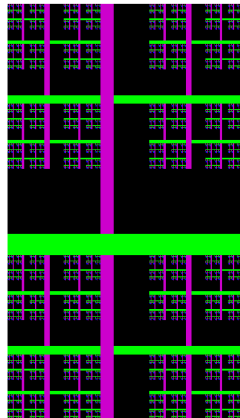
M-choose-N
perfect map



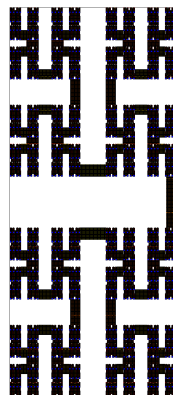
Linear
MR=2

DeHon March 2001

Area Comparison



M-choose-N
perfect map



Linear
MR=2

- Since
 - switch \gg wire
- may be able to tolerate $MR > 1$
- reduces switches
 - net area savings

DeHon March 2001

Multi-layer metal?

- Preceding assumed
 - fixed wire layers
- In practice,
 - increasing wire layers with shrinking tech.
 - Increasing wire layers with chip capacity
 - wire layer growth $\sim O(\log(N))$

DeHon March 2001

Multi-Layer

- Natural response to $\Omega(N^{2p})$ wire layers
 - Given N^p wires in bisection
 - rather than accept N^p width
 - use $N^{(p-0.5)}$ layers
 - accommodate in $N^{0.5}$ width
 - now wiring takes $\Omega(N)$ 2D area
 - with $N^{(p-0.5)}$ wire layers
 - for $p=0.5$,
 - $\log(N)$ layers to accommodate wiring

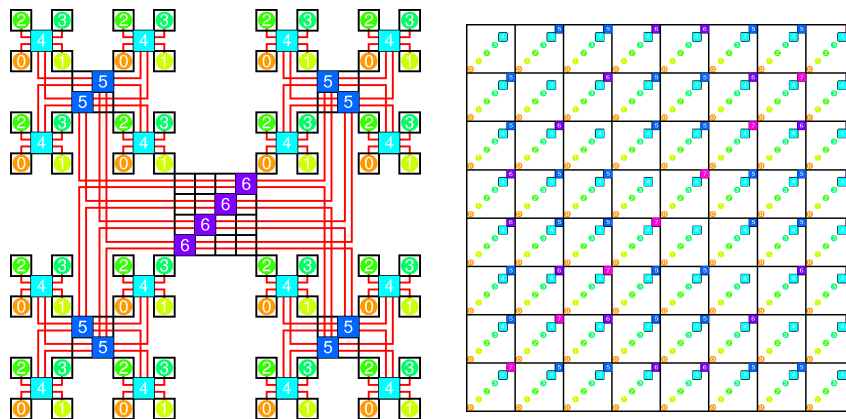
DeHon March 2001

Linear + Multilayer

- Multilayer says can do in $\Omega(N)$ 2D-area
- Switches require 2D-area
 - more than $O(N)$ switches would make switches dominate
 - Linear and Benes have $O(N)$ switches
- There's a possibility can achieve $O(N)$ area
 - with multilayer metal and linear population

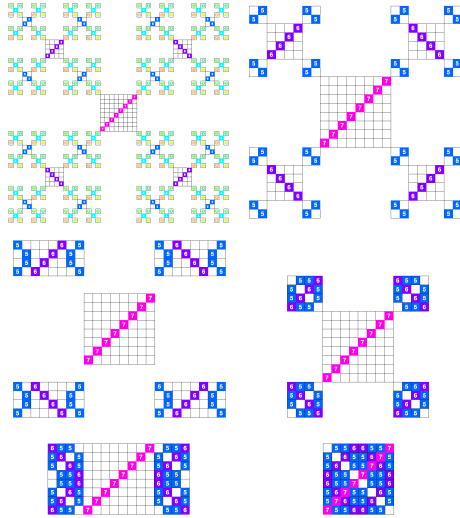
DeHon March 2001

Butterfly Fat-Tree Layout



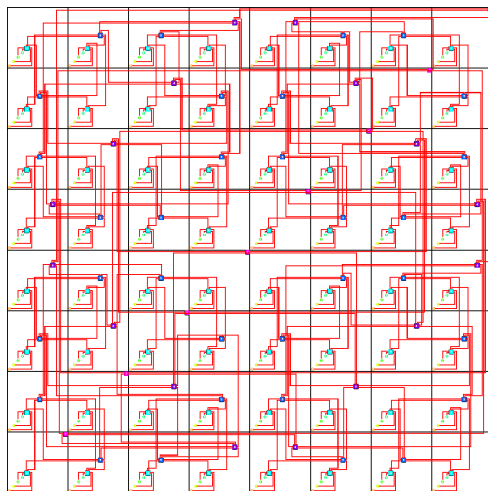
DeHon March 2001

Fold Sequence



DeHon March 2001

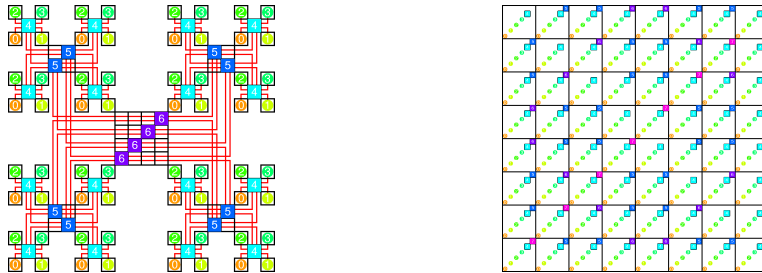
Compact, Multilayer BFT Layout



DeHon March 2001

Fold and Squash Result

- Can layout BFT
 - in $O(N)$ 2D area
 - with $O(\log(N))$ wiring layers



DeHon March 2001

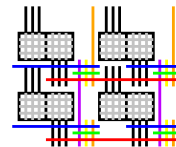
Summary

- Rent's Rule characterizes locality in design
- Exploiting that locality reduces
 - both wiring and switching requirements
- Naïve switches match wires at $O(N^{2p})$
 - switch area \gg wire area
 - prevent using multiple layers of metal
- Can achieve $O(N)$ switches
 - plausibly $O(N)$ area with sufficient metal layers

DeHon March 2001

Additional Information

- <http://www.cs.caltech.edu/research/ic/>



DeHon March 2001

Consider

- Crossbar case to exploit wiring:
 - split into two halves
 - $N/2 \times N/2$ crossbar each half
 - $N/2 \times (N/2)^p$ connect to bisection wires
 - $2 (1/4 N^2 + 1/2^{(p+1)} N^{(p+1)})$
 - $1/2 N^2 + 1/2^p N^{(p+1)} < N^2$

DeHon March 2001