ECE 252 / CPS 220
Advanced Computer Architecture I

Reading Discussion 1

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www.duke.edu/~bcl15
www.duke.edu/~bcl15/class/class_ece252fall11.html

ECE252 Administrivia

29 September – Homework #2 Due

- Use blackboard forum for questions
- Attend office hours with questions
- Email for separate meetings

Classic Machines…

Technology and Architecture

- Stored program computer and new memory
- Computation bottlenecks and new transistors

Racing Moore's Law

- Designs were outpaced by underlying technology
- Cray-1: Performance gain of 35% per year versus 60% in MOS scaling
- Cray-2: Performance gain of 13% per year versus 60% in MOS scaling

Rise of MOS Microprocessors

- Supercomputers used bipolar technologies with low volume
- Low volume implies less money for investment in bipolar technology
- Microprocessors used MOS technologies with high volume
- High volume implies more money for lithographic/device development

Cramming more components…

Moore's Law

- Number of transistors per chip double every year (2x / year)
- Corollary: Price per transistor decreases by a factor of two each year
- Corollary: Power and delay improve with scaling
- In practice, semiconductor technology improves (1.6x / year)

Forecasting

- Paper makes more than 25 predictions, all of which have come true
- Proliferation of computing into many areas (e.g., home, automobiles, portable communications, electronic wristwatches)
- Economics of market size and engineering costs and building large systems from standard components

The 801 Minicomputer

Co-Design of Compilers and ISAs

- Philosophy of basing the ISA on what a compiler needs
- Influenced Berkeley RISC and Stanford MIPS projects

Case for Software Subroutines

- More responsive systems as interrupts occur at instruction boundaries and instructions are simpler, shorter
- Optimizing compilers can re-organize instructions for performance
- "Wherever there is a system function that is expensive or slow in all its generality, but where software can recognize a frequently occurring degenerate case that function is moved from hardware to software, resulting in lower cost and improved performance"

The Case for RISC

RISC for General-Purpose Processors

- VLSI technology allowed more functionality per chip, providing significant performance gains
- Pipelining is a key technology to improve instruction rates and RISC architectures are more amenable to pipelining
- Most complex instructions are un-used.

Debate

- Started a RISC versus CISC debate in the 1980s
- Debate died down in the 1990s as semiconductor technology provided sufficient on-chip resources to allow high-performance CISC implementations

Instruction Sets and Beyond

Practical Rebuttal to RISC

- Technical elegance alone is insufficient in computer design
- Systems require upward compatibility and familiarity
- Designers benefit from well-defined, stable interface

Argument against All-or-None Approach

- Proposals for different approaches need not be segmented
- One side might easily adopt parts of a completely different proposal
- Example of windowed register file from Berkeley RISC that could be adopted by CISC processor if there were a need